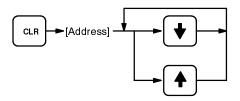
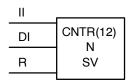
# SYSMAC C-series PCs Programming Instructions and Programming Console Operations

#### **Reference Manual**

Revised January 1993





#### Notice:

OMRON products are manufactured for use according to proper procedures by a qualified operator and only for the purposes described in this manual.

The following conventions are used to indicate and classify precautions in this manual. Always heed the information provided with them. Failure to head precautions can result in injury to people or damage to the product.

**DANGER!** Indicates information that, if not heeded, is likely to result in loss of life or serious

injury.

WARNING Indicates information that, if not heeded, could possibly result in loss of life or

serious injury.

Caution Indicates information that, if not heeded, could result in relative serious or minor

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#### **OMRON Product References**

All OMRON products are capitalized in this manual. The word "Unit" is also capitalized when it refers to an OMRON product, regardless of whether or not it appears in the proper name of the product.

The abbreviation "Ch," which appears in some displays and on some OMRON products, means "word" and is abbreviated "Wd" in documentation.

The abbreviation "PC" means Programmable Controller and is not used as an abbreviation for anything else.

#### Visual Aids

The following headings appear in the left column of the manual to help you locate different types of information.

**Note** Indicates information of particular interest for efficient and convenient operation of the product.

1, 2, 3... 1. Indicates lists of one sort or another, such as procedures, checklists, etc.

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#### About this Manual:

This Guide has been written to give users of C-series PCs a comprehensive reference for the programming instructions and Programming Console operations.

**Section 1** lists the Programming Console operations and the PCs for which they are applicable. It also gives a brief description of the function each operation performs.

**Section 2** gives a more detailed account of the implementation and effect of each operation, including the key sequence required to input it via the Programming Console. Operations are listed in the same order as they appear in the table of **Section 1**.

**Section 3** lists the full range of programming instructions, along with their function codes, names, mnemonics, and the PCs for which each is applicable. The tables in this section are listed alpha-numerically. Instructions without function codes are listed alphabetically first, followed by a numeric listing according to function codes. Block instructions have been kept separate and are listed numerically at the end of the section.

**Section 4** gives details on how the instructions are used. A detailed description of each instruction's function and processes is given, along with their ladder diagram symbols and the applicable data areas for the operands. This section has all entries listed in the same order as **Section 3**.

**Appendix A** provides a chart showing the Programming Console keys and their equivalent hexadecimal codes, for use with the KEY(62) instruction.

*Appendix B* lists the instructions according to the type of function they perform.

Appendix C provides an ASCII conversion chart.

Code

**Appendix D** provides a conversion chart that lists values in decimal, hexadecimal, binary, and binary-coded decimal.

The total range of SYSMAC C-series PCs referred to in this guide is as follows:

Applicable PCs

```
C20;
C20H, C28H, and C40H;
C20K, C28K, C40K, and C60K;
C20P, C28P, C40P, and C60P;
C120;
C200H;
C500; and
C1000H/C2000H
```

The codes in the Applicable PCs column in the of the tables describe the PC Units as follows:

	pp.::eu.o.
C_K:	C20K, C28K, C40K, and C60K
C_P:	C20P, C28P, C40P, and C60P
C_H:	C20H, C28H, and C40H, also known as Mini H-type
H-type PCs:	C20H, C28H, and C40H, C200H, and C1000H/C2000H

# SECTION 1 Summary of Console Operations and Applicable PCs

This section lists the Programming Console operations and the PCs for which they are applicable. The table gives the operation name, the function it performs, and the model numbers of the applicable PCs.

Name	Function	Applicable PCs
Password Input	Prompts the user for the access password.	All
Buzzer ON/OFF	Controls whether the buzzer will sound for keystroke inputs.	All but CP/CK
Data Clear	Used to erase data, either selectively or totally, from the Program Memory and the IR, AR, HR, DM, and TC areas.	All
I/O Table Register	Registers the I/O table after initial entry or subsequent amendments.	All but C20/C_P/C_K/ C_H
I/O Table Change	Allows dummy I/O words to be registered in the table so that the table does not need to be altered when the appropriate Units are added or removed.	C1000H/C2000H
Word Multiplier Enter	Used to assign word multipliers to Remote I/O Master Units.	C1000H/C2000H
I/O Table Verify	Checks the I/O Table against the actual arrangement of I/O Units.	All but C20/C_P/C_K/ C_H
I/O Table Read	Displays the Unit type, location, allocated I/O word, and word multiplier (where applicable).	All but C20/C_P/C_K/ C_H
I/O Table Transfer	Copies the I/O table to RAM. This enables simultaneous writing of the table and user program to EPROM.	C500/C1000H/C2000H
NET Link Link Table Transfer	Transfers a copy of the NET Link System's Link Table to the user memory (UM) area.	C200H-CPU11-E
I/O Table Delete	Deletes the entire I/O Table.	C200H/C500
On-line I/O Unit Change	Permissible Units can be mounted or removed while the CPU is operating.	C2000H
Program Header Display	Displays the program name, version number, and date of last revision.	C_H
Address Designation	Displays the specified address.	All
Program Input	Used to edit or input program instructions.	All
Program Read	Allows the user to scroll through the program address-by-address. In RUN and MONITOR modes, status of bits is also given.	All
Program Search	Searches a program for the specified data address or instruction.	All
Instruction Insert Instruction Delete	Allows a new instruction to be inserted before the displayed instruction, or deletes the displayed instruction (respectively).	All
Program Check	Checks the completed program for syntax errors (up to three levels in H-type PCs).	All
Debug Operation Enter	Enables special debugging operations to be performed.	C1000H/C2000H
Address Execution	Executes a program instruction-by-instruction starting from the current address.	C1000H/C2000H
Debug Execution	Debugs the program from the current address to the first END(01).	C1000H/C2000H
Address Trace	Traces up to 250 instructions from the program to the Trace Memory for use in debugging. Start address is specified by the trigger address and a positive or negative delay.	C1000H/C2000H
Address Trace Read	Reads data from the Trace Memory, starting from the trigger address.	C1000H/C2000H
Error Message Read	Displays error messages in sequence, starting with the most severe messages.	All
Bit/Word Monitor	Displays the specified address whose operand is to be monitored. In RUN or MONTR mode it will show the status of the operand for any bit or word in any data area.	All
3-word Monitor	Simultaneously monitors three consecutive words.	C200H/C1000H/C2000H/ CH
Forced Set/Reset	Set: Used to turn ON bits or timers, or to increment counters currently displayed on the left of the screen.  Reset: Used to turn OFF bits, or to reset timers or counters.	All
Clear Forced Set/Reset	Simultaneously clears all forced bits within the currently displayed word.	C200H/CH
Hex/BCD Data Change	Used to change the value of the leftmost BCD or hexadecimal word displayed during a Bit/Word Monitor operation.	All (for one scan only in C20/C_P/C_K)
Binary Data Change	Changes the value of 16-bit words bit-by-bit. Bits can be changed temporarily or permanently to the desired status.	All but C20/C_P/C_K
SV Change SV Reset	Alters the SV of a timer or counter either by incrementing or decrementing the value, or by overwriting the original value with a new one.	All

Name	Function	Applicable PCs
3-word Change	Used to change the value of a word displayed during a 3-word Monitor operation.	H-type
Scan Time Display	Measures the duration of the current scan. Scan times will vary according to the execution conditions which exist in each scan.	All but C20
Hex-ASCII Display Change	Converts 4-digit hexadecimal data in the DM area to ASCII and vice-versa.	H-type
Binary Monitor	Displays the monitored area in binary format.	H-type
Program Read-protect Clear	Clears protection set via instruction PPR(49).	СH
Program Memory Save	Saves Program Memory to tape.	All
Program Memory Restore	Reads Program Memory from tape.	All
Program Memory Compare	Compares Program Memory data on tape with that in the Program Memory area.	All
DM Data Save, Restore, Compare	The save, restore, and compare tape operations for DM area data.	All
PC to PROM Writer	Outputs Program Memory to the RS-232C interface for writing to a commercial PROM writer.	С_Н
PROM Writer to PC	Reads Program Memory data from a commercial PROM writer into the PC via the RS-232C interface.	С_Н
File Memory Clear	Clears memory, either selectively or totally, from the FM area.	C1000H/C2000H
File Memory Edit	Allows data in the FM area to be read and modified.	C1000H/C2000H
File Memory Read	Copies UM data from the FM area to a specified part of the Program Memory RAM, or IOM data in the FM area to one of the CPU data areas.	C1000H/C2000H
File Memory Write	Writes data from the Program Memory or data areas to the FM area.	C1000H/C2000H
File Memory Verify	Compares data in the FM area with that in the specified Program Memory or data areas.	C1000H/C2000H

# **SECTION 2**

# **Programming Console Operations**

This section lists the Programming Console operations according to their function. A brief description of each operation is given, along with the allowable modes in which it can be implemented, and the keystroke sequence used to enter it.

2-1	System Operations	6
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2-4	Monitoring and Data Changing Operations	12
2-5	Cassette Tape Operations	15
2-6	PROM Writer Operations	16
2-7	File Memory Operations	17

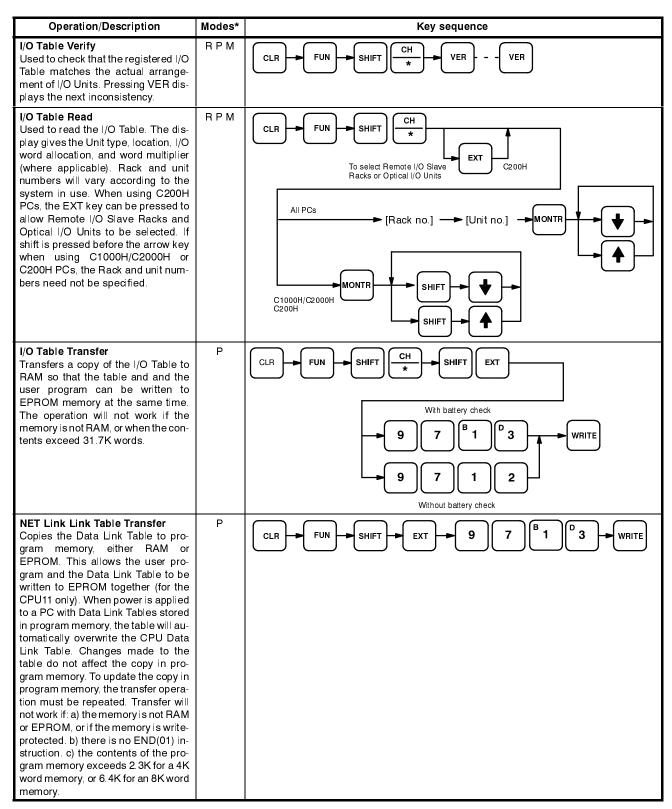
System Operations Section 2–1

# 2-1 System Operations

Operation/Description	Modes*	Key sequence
Password Input Controls access to the PC's programming functions. To gain access to the system once "PASSWORD" has been displayed, press CLR, MONTR, and then CLR.	RMP	CLR MONTR CLR
Buzzer ON/OFF The buzzer can be switched to operate whenever Programming Console keys are pressed (as well as for the normal error indication). BZ is displayed in the upper right corner when the buzzer is operative. The buzzer can be enabled by pressing SHIFT and then 1 immediately after entering the password, or after changing the mode.	RMP	SHIFT B 1
Data Clear Unless otherwise specified, this operation will clear all erasable memory in Program Memory and IR, HR, AR, DM, and TC areas. To clear EPROM memory the write enable switch must be ON (i.e., enabled). The branch lines shown are used only when performing a partial memory clear, with each of the memory areas entered being retained. Specifying an address will result in the Program Memory after and including that address being deleted. All memory up to that address will be retained.	P	CLR PLAY NOT RESET MONTR  [Address] Partial Clear  HR  CNT  Retained if pressed
I/O Table Register Whenever I/O Unit changes are made that affect the operation of the system, the I/O table needs to be corrected to reflect the changes. This includes the initial registration once the system has been established.	Э	CLR FUN SHIFT CHG 9 7 B 1 D 3 WRITE
I/O Table Change Allows I/O Units to be removed or added without the need to re-register the I/O Table or to amend the user program. By creating dummy entries, word address discrepancies can be avoided when the Units are added later.	P	I/O Table Read in progress  CHG  A 0  WRITE  I/O types  0: Output 1: Input 3: Word
Word Multiplier Enter If the system has Remote I/O Masters connected to I/O Link Units, Optical I/O Units, or Remote Terminals, a word multiplier must be assigned to each Master after the I/O table is registered. Word multipliers can take values from 0 to 3.	Р	I/O Table Register completed → [Word multiplier] → WRITE

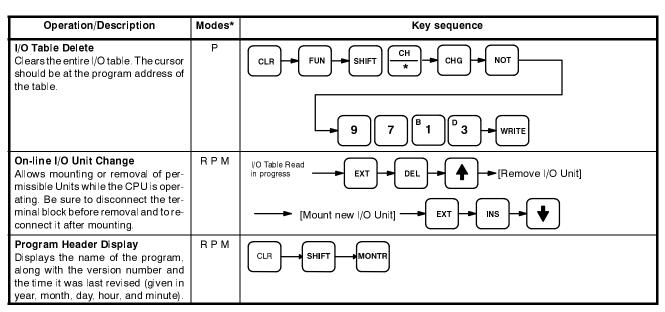
<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

System Operations Section 2–1



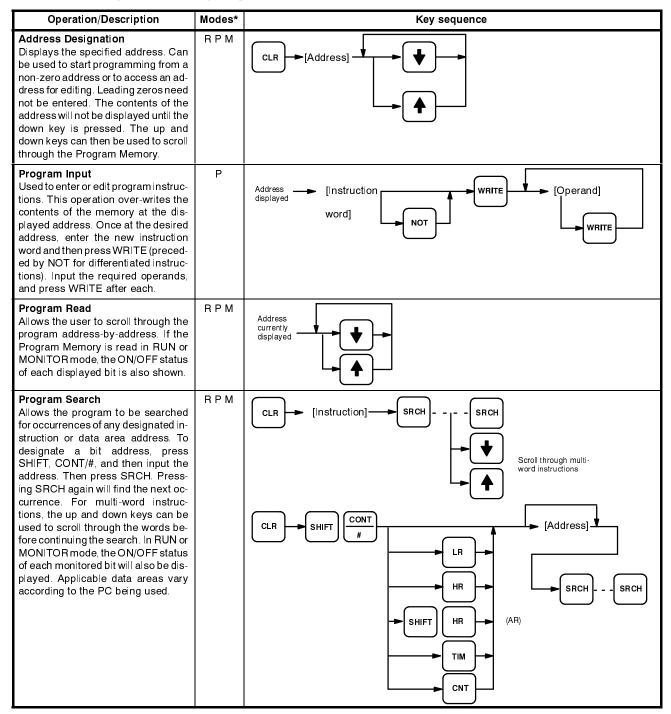
<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

System Operations Section 2–1

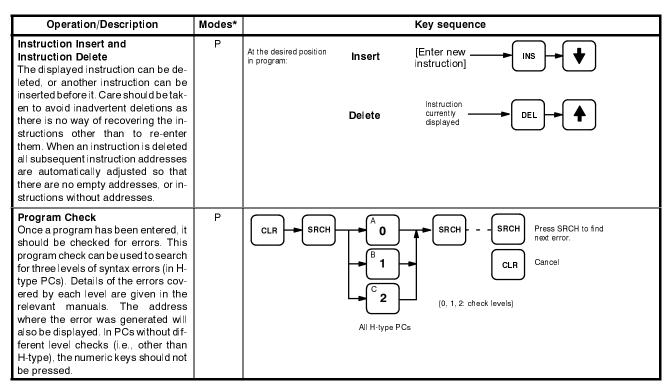


<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

#### 2-2 Programming Operations



<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM



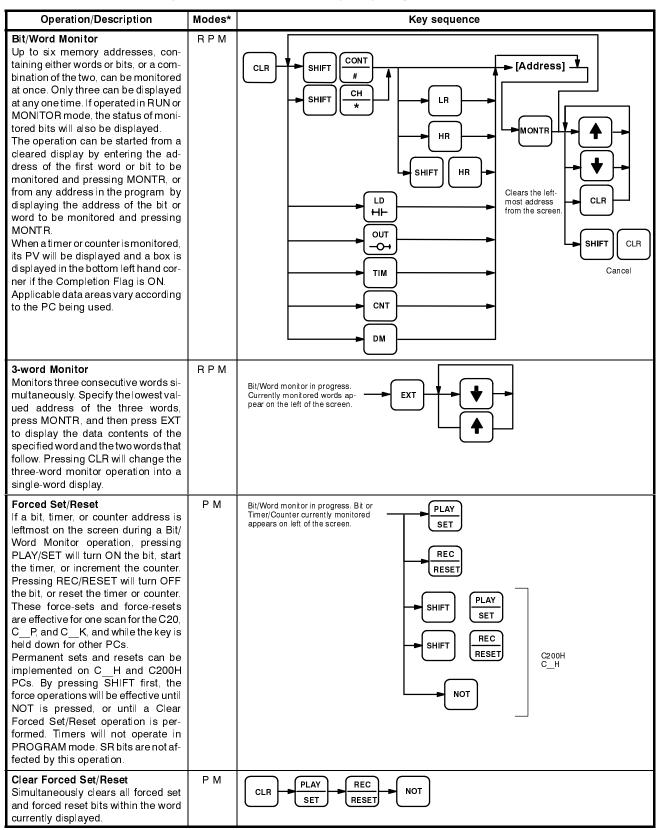
<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

# 2-3 Debugging Operations

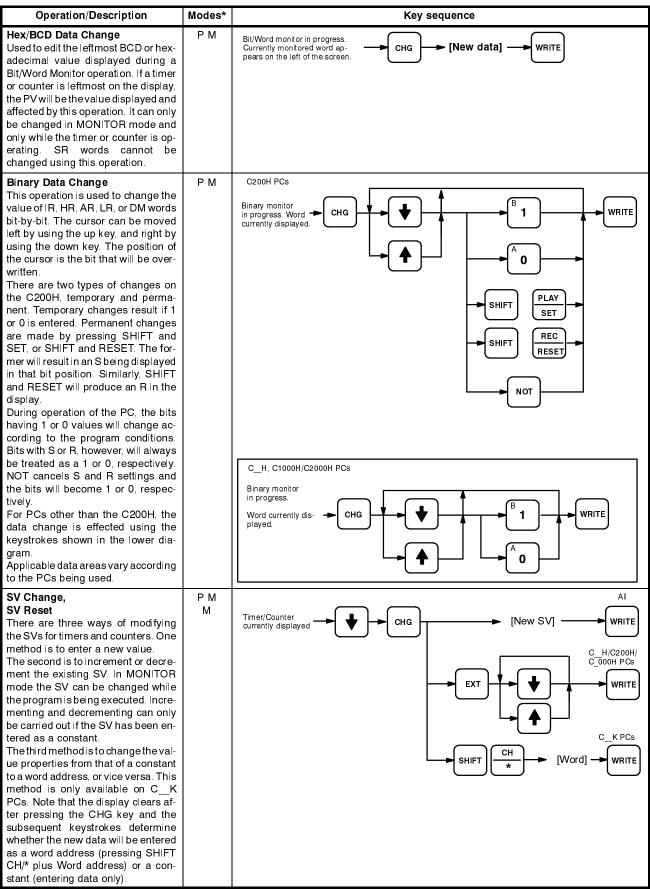
Operation/Description	Modes*	Key sequence
Debug Operation Enter Used to debug the program while in Program Mode. Program Input, Program Clear, Instruction Insert, and Instruction Delete operations are not available. Unless the Data Retention control bit is ON, all data in the IR, AR, and LR areas will be cleared when debug operation is entered or exited.	P	CLR SHIFT MONTR → Debug operation)  SHIFT MONTR (Debug operation → Program mode)
Address Execution Executes the program instruction-by- instruction starting from the current address. Press the down key to go to the next address. Word data can be monitored via the Data Monitor oper- ation.	P	Debug operation, current address  PLAY On  REC  RESET  Off
Debug Execution Executes the program from the current address to the specified stop address. Debugging will stop if END (01) is encountered, or if CLR is pressed.	Р	Debug operation EXT CHG Stop address ] CLR To cancel
Address Trace Traces up to 250 instructions from the program. Tracing begins at the address indicated by the trigger address and the delay. The delay can be in the range –249 to +250 (press NOT to toggle between – and +). Tracing continues up to the stop address, or until a maximum of 250 instruction words have been recorded. If END(01) is encountered, the tracing will loop back to the beginning address and continues until 250 words have been traced and recorded.	P	Debug operation  EXT  CHG  [Stop address]  WRITE  [Delay value]  CLR  To cancel
Address Trace Read Reads the Address Trace starting at the trigger address. The up and down arrow keys can be used to scroll through the instructions word-byword.	P	CLR MONTR +
Error Message Read Displays error messages in sequence with most severe messages displayed first. Press monitor to access remaining messages. In PROGRAM mode, pressing MONTR clears the displayed message from memory and the next message is displayed.	RPM	CLR FUN MONTR MONTR

<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

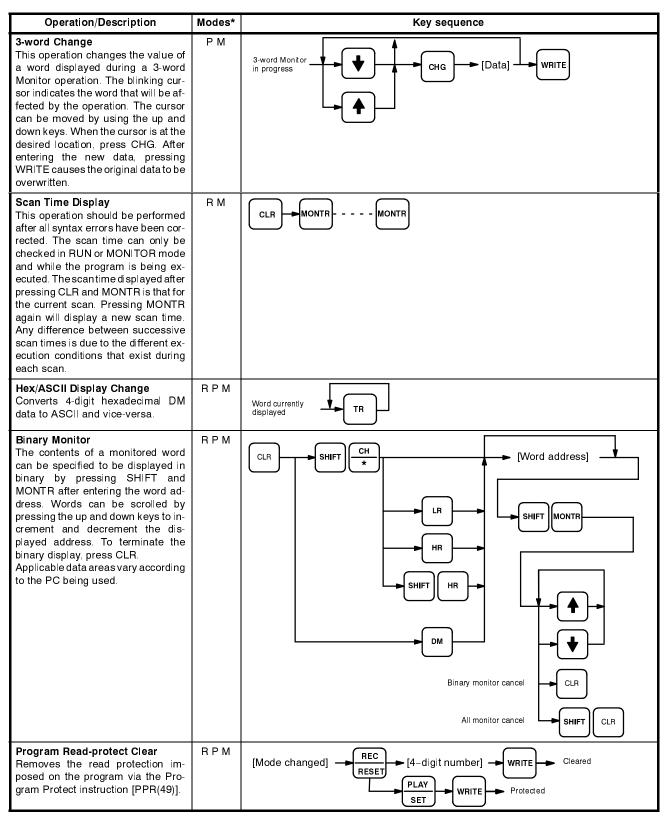
#### 2-4 Monitoring and Data Changing Operations



<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

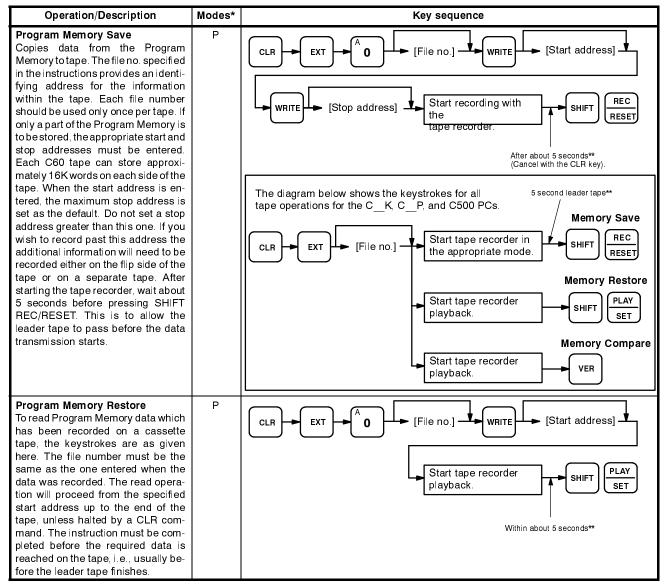


<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM



<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

### 2-5 Cassette Tape Operations



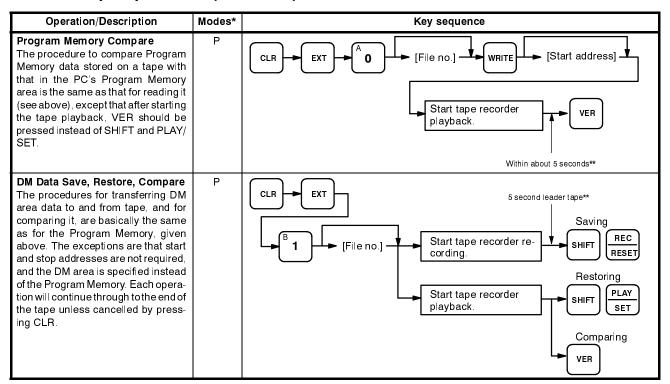
<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

<sup>\*\*</sup>These times take the cassette leader tape into consideration according to the following:

a) When recording to tape, the leader tape needs to be allowed to pass before the data transmission to the tape player starts.

b) When restoring from tape or comparing data, the Programming Console needs to be ready to receive data before the data is transfered from the tape.

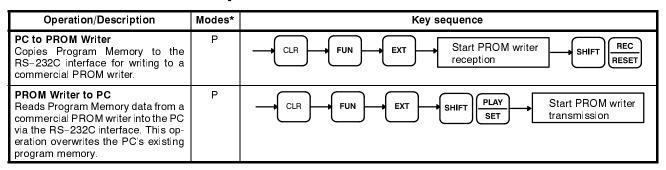
#### **Cassette Tape Operations (continued)**



<sup>\*\*</sup>These times take the cassette leader tape into consideration according to the following:

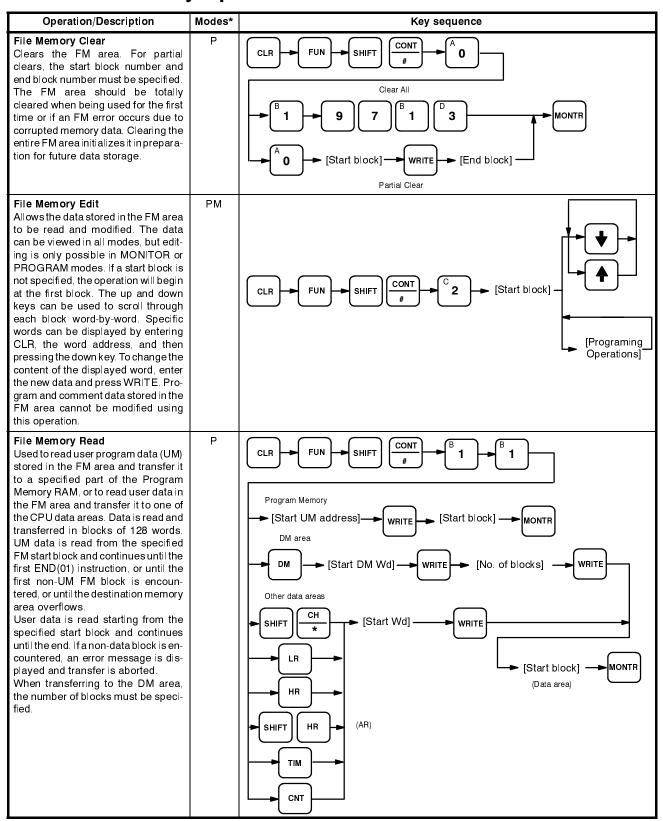
- a) When recording to tape, the leader tape needs to be allowed to pass before the data transmission to the tape player starts.
- b) When restoring from tape or comparing data, the Programming Console needs to be ready to receive data before the data is transferred from the tape.

#### 2-6 PROM Writer Operations

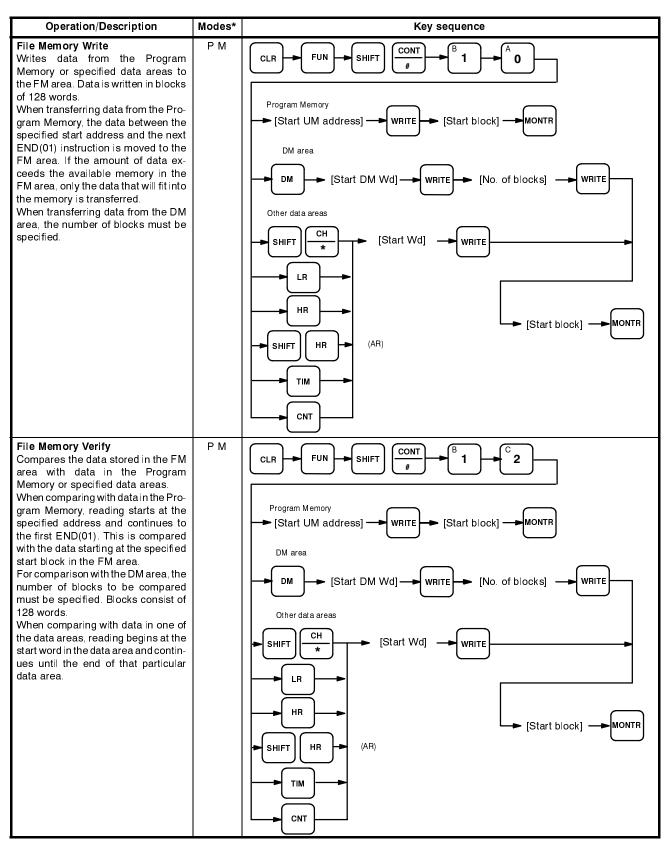


<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

#### 2-7 File Memory Operations



<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM



<sup>\*</sup>Modes in which the given instruction is applicable: R = RUN, M = MONITOR, P = PROGRAM

#### **SECTION 3**

# **Summary of Programming Instructions and Applicable PCs**

This section provides tables listing the full range of ladder diagram programming instructions used with C-series PCs. Section 3-1 summarizes all instructions other than block instructions. Section 3-2 lists the block instructions used with C1000H/C2000H PCs. In both tables, the entries are listed alphanumerically. Instructions without function codes are given first in alphabetical order, according to the mnemonic. These are followed by the instructions with function codes which are listed numerically, according to the function code. Appendix B lists the instructions in groups according to the type of function they perform.

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Standard Instructions Section 3–1

#### 3-1 Standard Instructions

The following table lists the standard programming instructions available for C-series PCs. A PC instruction is entered either using the appropriate Programming Console key(s) (e.g., LD, AND, OR, NOT), or by using function codes. To input an instruction using its function code, press FUN, the function code, and then WRITE.

Function Code	Name	Mnemonic	Applicable PCs
	AND	AND	All
	AND LOAD	AND LD	All
	AND NOT	AND NOT	All
	COUNTER	CNT	All
	LOAD	LD	All
	LOAD NOT	LD NOT	All
	OR	OR	All
	OR LOAD	OR LD	All
	OR NOT	OR NOT	All
	OUTPUT	OUT	All
	OUTPUT NOT	OUT NOT	All but C20
	TIMER	TIM	All
00	NO OPERATION	NOP	All
01	END	END	All
02	INTERLOCK	IL	All
03	INTERLOCK CLEAR	ILC	All
04	JUMP	JMP	All but C20
05	JUMP END	JME	All but C20
06	FAILURE ALARM	FAL	All but C20/C_P/C_K
07	SEVERE FAILURE ALARM	FALS	All but C20/C_P/C_K
08	STEP DEFINE	STEP	C_K/C_H/C200H/C_000H
09	STEP START	SNXT	C_K/C_H/C200H/C_000H
10	SHIFT REGISTER	SFT	All
11	KEEP	KEEP	All
12	REVERSIBLE COUNTER	CNTR	All but C20
13	DIFFERENTIATE UP	DIFU	All
14	DIFFERENTIATE DOWN	DIFD	All
15	HIGH-SPEED TIMER	TIMH	All
16	WORD SHIFT	WSFT	All but C20
17	REVERSIBLE WORD SHIFT	RWS	C20H/C28H/C40H/C200H
18	SCAN TIME	SCAN	C20H/C28H/C40H/C200H
19	MULTI-WORD COMPARE	MCMP	C200H
20	COMPARE	CMP	All
21	MOVE	MOV	All
22	MOVE NOT	MVN	All
23	BCD-TO-BINARY	BIN	All but C20
24	BINARY-TO-BCD	BCD	All but C20
25	ARITHMETIC SHIFT LEFT	ASL	All but C20/C_P/C_K
26	ARITHMETIC SHIFT RIGHT	ASR	All but C20/C_P/C_K
27	ROTATE LEFT	ROL	All but C20/C_P/C_K
28	ROTATE RIGHT	ROR	All but C20/C_P/C_K

Standard Instructions Section 3–1

Function Code	Name	Mnemonic	Applicable PCs
29	COMPLEMENT	СОМ	All but C20/C_P/C_K
30	BCD ADD	ADD	All
31	BCD SUBTRACT	SUB	All
32	BCD MULTIPLY	MUL	All but C20/C_P
33	BCD DIVIDE	DIV	All but C20/C_P
34	LOGICAL AND	ANDW	All but C20/C_P/C_K
35	LOGICAL OR	ORW	All but C20/C_P/C_K
36	EXCLUSIVE OR	XORW	All but C20/C_P/C_K
37	EXCLUSIVE NOR	XNRW	All but C20/C_P/C_K
38	INCREMENT	INC	All but C20/C_P/C_K
39	DECREMENT	DEC	All but C20/C_P/C_K
40	SET CARRY	STC	All
41	CLEAR CARRY	CLC	All
42	FILE MEMORY READ	FILR	C1000H/C2000H
43	FILE MEMORY WRITE	FILW	C1000H/C2000H
44	EXTERNAL PROGRAM READ	FILP	C1000H/C2000H
45	TRACE MEMORY SAMPLE	TRSM	C1000H/C2000H
46	DISPLAY MESSAGE	MSG	C200H/C1000H/C2000H
47	LONG MESSAGE	LMSG	C20H/C28H/C40H/C200H
48	TERMINAL MODE	TERM	C200H
49	PROGRAM PROTECT	PPR	C200H
49	SET SYSTEM	SYS	C20H/C28H/C40H
50	BINARY ADD	ADB	C200H/C1000H/C2000H
51	BINARY SUBTRACT	SBB	C200H/C1000H/C2000H
52	BINARY MULTIPLY	MLB	C200H/C1000H/C2000H
53	BINARY DIVIDE	DVB	C200H/C1000H/C2000H
54	DOUBLE BCD ADD	ADDL	C200H/C1000H/C2000H
55	DOUBLE BCD SUBTRACT	SUBL	C200H/C1000H/C2000H
56	DOUBLE BCD MULTIPLY	MULL	C200H/C1000H/C2000H
57	DOUBLE BCD DIVIDE	DIVL	C200H/C1000H/C2000H
58	DOUBLE BCD-TO-DOUBLE BINARY	BINL	C200H/C1000H/C2000H
59	DOUBLE BINARY-TO-DOUBLE BCD	BCDL	C200H/C1000H/C2000H
60	DOUBLE COMPARE	CMPL	C200H
60	REVERSIBLE DRUM COUNTER	RDM	C_K/C20H/C28H/C40H
61	HIGH-SPEED DRUM COUNTER	HDM	C20H/C28H/C40H/CK (for CP, see function code 98)
62	KEY INPUT	KEY	C20H/C28H/C40H
62	END WAIT	ENDW	С_К
63	COLUMN-TO-WORD	CTW	C200H
63	NOTATION INSERT	NETW	С_К
64	WORD-TO-COLUMN	WTC	C200H
65	HOURS-TO-SECONDS	HTS	C20H/C28H/C40H/C200H
66	SECONDS-TO-HOURS	STH	C20H/C28H/C40H/C200H
67	BIT COUNTER	BCNT	C_H/C200H/C_000H
68	BLOCK COMPARE	ВСМР	CH/C200H/C_000H
69	VALUE CALCULATE	VCAL	C200H

Standard Instructions Section 3–1

Function Code	Name	Mnemonic	Applicable PCs
70	BLOCK TRANSFER	XFER	All but C20/C_P/C_K
71	BLOCK SET	BSET	All but C20/C_P/C_K
72	SQUARE ROOT	ROOT	All but C20/C_P/C_K/C_H
73	DATA EXCHANGE	XCHG	All but C20/C_P/C_K
74	ONE DIGIT SHIFT LEFT	SLD	All but C20/C_P/C_K/C_H
75	ONE DIGIT SHIFT RIGHT	SRD	All but C20/C_P/C_K/C_H
76	4-TO-16 DECODER	MLPX	All but C20
77	16-TO-4 ENCODER	DMPX	All but C20
78	7-SEGMENT DECODER	SDEC	All but C20/C_P/C_K/C_H
79	FLOATING POINT DIVIDE	FDIV	All but C20/C_P/C_K/C_H
80	SINGLE WORD DISTRIBUTE	DIST	All but C20/C_P/C_K/C_H/C200H
81	DATA COLLECT	COLL	All but C20/C_P/C_K/C_H/C200H
82	MOVE BIT	MOVB	All but C20/C_P/C_K
83	MOVE DIGIT	MOVD	All but C20/C_P/C_K/C_H
84	REVERSIBLE SHIFT REGISTER	SFTR	All but C20/C_P
85	TABLE COMPARE	TCMP	All but C20/C_P/C_K/C_H
86	ASCII CONVERT	ASC	C200H/C1000H/C2000H
87	I/O WRITE	WRIT	C120/C500/C1000H/C2000H
88	I/O READ	READ	C120/C500/C1000H/C2000H
89	INTERRUPT CONTROL	INT	C200H/C1000H/C2000H
90	NETWORK SEND	SEND	C500/C1000H/C2000H/C200H (CPU11)
91	SUBROUTINE ENTER	SBS	All but C20/C_P*
92	SUBROUTINE START	SBN	All but C20/C_P*
93	RETURN	RET	All but C20/C_P*
94	WATCHDOG TIMER REFRESH	WDT	All but C20/C_P/C_K
96	BLOCK PROGRAM START	BPRG	C1000H/C2000H
97	I/O REFRESH	IORF	All but C20/C_P
98	NETWORK RECEIVE	RECV	C500/C1000H/C2000H/C200H (CPU11)
98	HIGH-SPEED DRUM COUNTER	HDM	C_P (for C20H/C28H/C40H/C_K, see function code 61)
99	RUN STOP	STOP	C120

<sup>99</sup> RUN STOP STOP

\*C120 and C500: High-speed scan models only. See function codes 91, 92 and 93

Block Instructions Section 3–2

#### 3-2 Block Instructions

Block instructions can be used for block programming on C1000H/C2000H PCs. The pointed parenthesis, ke this>, indicates that the instruction is a block programming instruction and that, in order for the PC to be able to distinguish between it and the basic instruction with the same number, SHIFT must be pressed before keying in the function code.

Function Code	Name	Mnemonic	Applicable PCs
<01>	BLOCK PROGRAM END	BEND	C1000H/C2000H
<02>	CONDITIONAL BRANCH	IF	C1000H/C2000H
<03>	NO BRANCH	ELSE	C1000H/C2000H
<04>	BRANCH END	IEND	C1000H/C2000H
<05>	ONE SCAN AND WAIT	WAIT	C1000H/C2000H
<06>	CONDITIONAL BLOCK EXIT	EXIT	C1000H/C2000H
<07>	SET	SET	C1000H/C2000H
<08>	RESET	RSET	C1000H/C2000H
<09>	LOOP	LOOP	C1000H/C2000H
<10>	LOOP END	LEND	C1000H/C2000H
<11>	BLOCK PROGRAM PAUSE	BPPS	C1000H/C2000H
<12>	BLOCK PROGRAM RESTART	BPRS	C1000H/C2000H
<13>	TIMER WAIT	TIMW	C1000H/C2000H
<14>	COUNTER WAIT	CNTW	C1000H/C2000H
<15>	HIGH-SPEED TIMER WAIT	TMHW	C1000H/C2000H

#### **SECTION 4**

# **Programming Instructions**

The following tables detail all ladder diagram programming instructions and the applicable data areas for each. Remember that not all PCs provide all of the data areas. Bit and word addresses for each area in each PC are given in the footnotes at the bottom of the page. This information is spread over two pages.

Differentiated instructions (indicated with @) are entered by pressing the NOT key on the Programming Console following the function code.

The DM area can be indirectly addressed by specifying the data area as \*DM, and then entering the address of the DM word that contains the actual data.

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Basic Instructions Section 4–1

## 4-1 Basic Instructions

Name Mnemonic	Symbol	Function	Operand Data Areas
AND AND	B —— <b> </b>  ——	Logically ANDs the status of the designated bit with the current execution condition.	B: IR SR HR AR LR TC
AND LOAD AND LD		Logically ANDs the resultant execution conditions of the preceding logic blocks.	None
AND NOT AND NOT	B <del>}/}-</del> -	Logically ANDs the inverse of the designated bit with the current execution condition.	B: IR SR HR AR LR TC
COUNTER CNT	CP CNT N R SV	A decrementing counter. SV: 0 to 9999; CP: count pulse; R: reset input. The TC bit is entered as a constant.	N: SV: TC IR HR AR LR DM #
<b>LOAD</b> LD	B B	Defines the status of bit B as the execution condition for subsequent operations in the instruction line.	B: IR SR HR AR LR TC TR
LOAD NOT LD NOT	B #	Defines the status of the inverse of bit B as the execution condition for subsequent operations in the instruction line.	B: IR SR HR AR LR TC
<b>OR</b> OR	B	Logically ORs the status of the designated bit with the current execution condition.	B: IR SR HR AR LR TC

**Data Areas:** These footnote tables show the bit addresses (word addresses are given for DM and TC) of all data areas for each PC. To change bit addresses to word addresses, remove the rightmost two digits for word addresses.

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Basic Instructions Section 4–1

Name Mnemonic	Symbol	Function	Operand Data Areas
<b>OR LOAD</b> OR LD	+41 <u>1</u> 1+	Logically ORs the resultant execution conditions of the preceding logic blocks.	None
OR NOT OR NOT		Logically ORs the inverse of the designated bit with the execution condition.	B: IR SR HR AR LR TC
<b>OUTPUT</b> OUT	B	Turns ON B for an ON execution condition; turns OFF B for an OFF execution condition.	B: IR SR HR AR LR TR
OUT NOT OUT NOT	B	Turns OFF B for an ON execution condition; turns ON B for an OFF execution condition.	B: IR SR HR AR LR
TIMER TIM	TIM N	ON-delay (decrementing) timer operation. Set value: 000.0 to 999.9 s. The same TC bit cannot be assigned to more than one timer/counter. The TC bit is entered as a constant.	N: SV: TC IR HR AR LR DM #

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Special Instructions Section 4–2

# 4-2 Special Instructions

Name Mnemonic	Symbol	Function	Operand Data Areas
NO OPERATION NOP(00)	None	Nothing is executed and program operation moves to the next instruction.	None
END END(01)	—— END(01)	Required at the end of each program. Instructions located after END(01) will not be executed.	None
INTERLOCK IL(02) INTERLOCK CLEAR ILC(03)	——————————————————————————————————————	If an interlock condition is OFF, all outputs and all timer PVs between the current IL(02) and the next ILC(03) are turned OFF or reset, respectively. Other instructions are treated as NOP. Counter PVs are maintained. If the execution condition is ON, execution continues normally.	None
JUMP JMP(04) JUMP END JME(05)	— JMP(04) N — JME(05) N	When the execution condition for the JMP(04) instruction is ON, all instructions between JMP(04) and the corresponding JME(05) are to be ignored or treated as NOP(00). For direct jumps, the corresponding JMP(04) and JME(05) instructions have the same N value in the range 01 through 99. Direct jumps are usable only once each per program (i.e., N is 01 through 99 can be used only once each) and the instructions between the JUMP and JUMP END instructions are ignored; 00 may be used as many times as necessary, instructions between JMP 00 and the next JME 00 are treated as NOP, thus increasing scan time, as compared with direct jumps. N is not required with C_K, C_P, C120 and C500 PCs; the corresponding JME(05) is the next one in the program, with instructions between JMP(04) and JME(05) treated as NOP(00). There is no limit to the number of jumps in C120 and C500 programs. C_K and C_P programs may have a maximum of 8 JMP(04)/JME(05) pairs.	N: 00 to 99 (not applicable for C_P, C_K, or C120 PCs)
FAILURE ALARM (@)FAL(06)	—— FAL(06) N	Assigns a failure alarm code to the given execution condition. When N can be given a value between 01 and 99 to indicate that a non-fatal error (i.e., one that will not stop the CPU) has occurred. This is indicated by the PC outputting N (the FAL number) to the FAL output area. To reset the FAL area, N can be defined as 00. This will cause all previously recorded FAL numbers in the FAL area to be deleted. FAL data sent after a 00 will be recorded in the normal way. The same code numbers can be used for both FAL(06) and FALS(07).	<b>N:</b> 00 to 99

**Data Areas:** These footnote tables show the bit addresses (word addresses are given for DM and TC) of all data areas for each PC. To change bit addresses to word addresses, remove the rightmost two digits for word addresses.

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Section 4-2

Name Mnemonic	Symbol	Function	Operand Data Areas
SEVERE FAILURE ALARM FALS(07)	FALS(07) N	A fatal error is indicated by outputting N to the FAL output area and the CPU is stopped. The same FAL numbers are used for both FAL(06) and FALS(07).	<b>N</b> : 01 to 99
STEP DEFINE STEP(08)	STEP(08) B	When used with a control bit (B), defines the start of a new step and resets the previous step. When used without B, it defines the end of step execution.	B: IR HR AR LR
STEP START SNXT(09)	SNXT(09) B	Used with a control bit (B) to indicate the end of the step, reset the step, and start the next step which has been defined with the same control bit	B: IR HR AR LR
SHIFT REGISTER SFT(10)	P   SFT(10)   St   E	Creates a bit shift register for data from the starting word (St) through to the ending word (E). I: input bit; P: shift pulse; R: reset input. St must be less than or equal to E. St and E must be in the same data area.	St/E: IR HR AR LR
		15 00 15 00 E St N	
KEEP KEEP(11)	S KEEP(11) R B	Defines a bit (B) as a latch, controlled by the set (S) and reset (R) inputs.	B: IR HR AR LR
REVERSIBLE COUNTER CNTR (12)	DI CNTR(12) R SV	Increases or decreases the PV by one whenever the increment input (II) or decrement input (DI) signals, respectively, go from OFF to ON. SV: 0 to 9999; R: reset input. Each TC bit can be used for one timer/counter only. The TC bit is entered as a constant.	N: SV: TC IR SR HR AR LR DM #
DIFFERENTIATE UP DIFU(13) DIFFERENTIATE DOWN DIFD(14)	— DIFU(13) B — DIFD(14) B	DIFU(13) turns ON the designated bit (B) for one scan on reception of the leading (rising) edge of the input signal; DIFD(14) turns ON the bit for one scan on reception of the trailing (falling) edge.	B: IR HR AR LR
HIGH-SPEED TIMER TIMH(15)	TIMH(15) N	A high-speed, ON-delay (decrementing) timer. SV: 00.02 to 99.99 s. Each TC bit can be assigned to only one timer or counter. The TC bit is entered as a constant.	N: SV: TC IR SR HR AR LR HR

Special Instructions

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
WORD SHIFT (@)WSFT(16)	WSFT(16) St E	The data in the words from the starting word (St) through to the ending word (E), is shifted left in word units, writing all zeros into the starting word. St must be less than or equal to E, and St and E must be in the same data area.	St/E: IR HR AR LR DM
REVERSIBLE WORD SHIFT (@)RWS(17) (CPU11)	RWS(17) C St E	Creates and controls a reversible non-synchronous word shift register between St and E. Exchanges the content of a word containing zero with the content of either the preceding or following word, depending on the shift direction. Bits 13, 14, and 15 of control word C determine the mode of operation of the register according to the following: The shift direction is determined by bit 13 (OFF shifts the non-zero data to higher addressed words; ON to lower addressed words). Bit 14 is the register enable bit (ON for shift enabled). Bit 15 is the reset bit (if bit 15 is ON, the register will be set to zero between St and E when the instruction is executed with bit 14 also ON). St and E must be in the same data area.	C: St/E: IR IR SR SR HR HR AR AR LR LR TC TC DM DM #
SCAN TIME (@)SCAN(18) (CPU11)	SCAN(18)  Mi	Sets the minimum scan time, Mi, in tenths of milliseconds. The possible setting range is from 0 to 999.0 ms. If the actual scan time is less than the time set using SCAN(18), the CPU will wait until the designated time has elapsed before starting the next scan.	Mi:: IR Not used. SR HR AR LR TC DM #
MULTI-WORD COMPARE (@)MCMP(19) (CPU11)	MCMP(19) S <sub>1</sub> S <sub>2</sub> D	Compares the data within a block of 16 words of 4-digit hexadecimal data ( $S_1$ to $S_1$ +15) with that in another block of 16 words ( $S_2$ to $S_2$ +15) on a word-by-word basis. If the words are not in agreement, the bit corresponding to unmatched words turns ON in the result word, D. Bits corresponding to words that are equal are turned OFF.	S <sub>1</sub> /S <sub>2</sub> : D: IR IR SR SR HR HR AR LR TC TC DM DM
COMPARE (@)CMP(20)		Compares the data in two 4-digit hexadecimal words (Cp1 and Cp2) and outputs result to the GR, EQ, or LE Flags.	Cp1/Cp2: IR SR HR AR LR TC DM #

**Data Areas:** These footnote tables show the bit addresses (word addresses are given for DM and TC) of all data areas for each PC. To change bit addresses to word addresses, remove the rightmost two digits for word addresses.

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Special Instructions Section 4–2

Name Mnemonic	Symbol	Function	Operand Data Areas
MOVE (@)MOV(21)		Transfers data from source word, (S) to destination word (D).	S: D: IR IR SR HR HR AR LR LR DM TC DM #
MOVE NOT (@)MVN(22)	MVN(22) S D	Transfers the inverse of the data in the source word (S) to destination word (D).	S: D: IR IR SR HR HR AR LR LR DM TC DM #
BCD-TO-BINARY (@)BIN(23)	BIN(23) S R	Converts 4-digit, BCD data in source word (S) into 16-bit binary data, and outputs converted data to result word (R).  S (BCD)  X100  X101  X160  X161  X162  X103  X163	S: R: IR IR SR HR HR AR AR LR LR DM TC DM
BINARY-TO-BCD (@)BCD(24)	BCD(24) S R	Converts binary data in source word (S) into BCD, and outputs converted data to result word (R).  S (BIN)  X160  X161  X161  X162  X102  X103	S: R: IR IR SR HR HR AR LR DM DM
ARITHMETIC SHIFT LEFT (@)ASL(25)	ASL(25) Wd	Each bit within a single word of data (Wd) is shifted one bit to the left, with zero written to bit 00 and bit 15 moving to CY.  15 00  CY Wd 0	Wd: IR HR AR LR DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
ARITHMETIC SHIFT RIGHT (@)ASR(26)	——————————————————————————————————————	Each bit within a single word of data (Wd) is shifted one bit to the right, with zero written to bit 15 and bit 00 moving to CY.	Wd: IR HR AR LR DM
ROTATE LEFT (@)ROL(27)		Each bit within a single word of data (Wd) is moved one bit to the left, with bit 15 moving to carry (CY), and CY moving to bit 00.	Wd: IR HR AR LR DM
ROTATE RIGHT (@)ROR(28)	ROR(28) Wd	Each bit within a single word of data (Wd) is moved one bit to the right, with bit 00 moving to carry (CY), and CY moving to bit 15.	Wd: IR HR AR LR DM
COMPLEMENT (@)COM(29)		Inverts bit status of one word (Wd) of data, changing 0s to 1s, and vice versa.  Wd - Wd	Wd: IR HR AR LR DM
BCD ADD (@)ADD(30)	ADD(30) Au Ad R	Adds two 4-digit BCD values (Au and Ad) and content of CY, and outputs the result to the specified result word (R).  Au + Ad + CY - R CY	Au/Ad: R: IR IR SR HR HR AR LR LR DM TC DM #
BCD SUBTRACT (@)SUB(31)	SUB(31) Mi Su R	Subtracts both the 4-digit BCD subtrahend (Su) and content of CY, from the 4-digit BCD minuend (Mi) and outputs the result to the specified result word (R).  Mi – Su – CY R CY	Mi/Su: R: IR IR SR HR HR AR LR LR DM TC DM #
BCD MULTIPLY (@)MUL(32)	MUL(32)  Md  Mr  R	Multiplies the 4-digit BCD multiplicand (Md) and 4-digit BCD multiplier (Mr), and outputs the result to the specified result words (R and R + 1). R and R + 1 must be in the same data area.  Md x Mr R + 1 R	Md/Mr: R: IR IR SR HR HR AR LR LR DM TC DM #

Data Areas: These footnote tables show the bit addresses (word addresses are given for DM and TC) of all data areas for each PC. To change bit addresses to word addresses, remove the rightmost two digits for word addresses.

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
BCD DIVIDE (@)DIV(33)	DIV(33) Dd Dr R	Divides the 4-digit BCD dividend (Dd) by the 4-digit BCD divisor (Dr), and outputs the result to the specified result words. R receives the quotient; R + 1 receives the remainder. R and R + 1 must be in the same data area.  Dd ÷ Dr • R + 1	Dd/Dr: R: IR IR SR HR HR AR LR LR DM TC DM #
LOGICAL AND (@)ANDW(34)	ANDW(34) 11 12 R	Logically ANDs two 16-bit input words (I1 and I2) and sets the bits in the result word (R) if the corresponding bits in the input words are both ON.	I1/I2: R: IR IR SR HR HR AR LR LR DM TC DM #
LOGICAL OR (@)ORW(35)	ORW(35)  11  12  R	Logically ORs two 16-bit input words (I1 and I2) and sets the bits in the result word (R) when one or both of the corresponding bits in the input words is/are ON.	I1/I2: R: IR IR SR HR HR AR AR LR LR DM TC DM #
EXCLUSIVE OR (@)XORW(36)	XORW(36)  11  12  R	Exclusively ORs two 16-bit input words (I1 and I2) and sets the bits in the result word (R) when the corresponding bits in input words differ in status.	I1/I2: R: IR IR SR HR HR AR LR LR DM TC DM #
EXCLUSIVE NOR (@)XNRW(37)	XNRW(37) 11 12 R	Exclusively NORs two 16-bit input words (I1 and I2) and sets the bits in the result word (R) when the corresponding bits in both input words have the same status.	
INCREMENT (@)INC(38)	INC(38) Wd	Increments the value of a 4-digit BCD word (Wd) by one, without affecting carry (CY).	Wd: IR HR AR LR DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
DECREMENT (@)DEC(39)	DEC(39) Wd	Decrements the value of a 4-digit BCD word by 1, without affecting carry (CY).	Wd: IR HR AR LR DM
SET CARRY (@)STC(40)	—— STC(40)	Sets the Carry Flag (i.e., turns CY ON).	None
CLEAR CARRY (@)CLC(41)	—— CLC(41)	Clears the Carry Flag (i.e, turns CY OFF).	None
FILE MEMORY READ (@)FILR(42)	FILR(42)  N S D	Reads data from the File Memory area in 128-word block units, and outputs data to the specified PC destination words. N gives the number of blocks to be transferred. S specifies the starting source block. D specifies the address of the starting destination word.  PC memory  File memory  S  S+N-1	N/S: D: IR IR SR HR HR AR AR LR LR TC TC DM DM #
FILE MEMORY WRITE (@)FILW(43)	FILW(43)  N S D	Transfers data from the PC memory area to the File Memory area in 128-word (block) units. N gives the number of blocks to be transferred. S specifies the address of the starting source word. D gives the address of the starting destination block  PC memory  File memory  D  D+N-1	

**Data Areas:** These footnote tables show the bit addresses (word addresses are given for DM and TC) of all data areas for each PC. To change bit addresses to word addresses, remove the rightmost two digits for word addresses.

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
EXTERNAL PROGRAM READ (@)FILP(44)	FILP(44) BB	Copies program data from the File Memory blocks between the beginning block number (BB) and the first END(01), and transfers it to Program Memory area at the addresses immediately following FLIP(44). The transferred program is then executed.  PC memory File Memory  BB  END	BB: IR SR HR AR LR TC DM #
TRACE MEMORY SAMPLE TRSM(45)	—— TRSM(45)	Initiates data tracing. Used in conjunction with flags in the AR area to simplify debugging. Parameters are set using the Address Trace operation on a Programming Console or other System Support Tool (e.g., FIT, GPC, or LSS). AR 1815 starts sampling, AR 1814 starts the recording of the samples which are written to the Trace Memory of the GPC, FIT, or LSS. A positive or negative delay can be set for the recording of the samples. AR 1813 and 1812 indicate tracing in progress and tracing complete, respectively.	None
DISPLAY MESSAGE (@)MSG(46)	MSG(46) FM	Displays eight words of ASCII code, starting from FM, on the Programming Console or GPC. All eight words must be in the same data area.  FM A B C D  FM+ 7 D P  ABCDDP	FM: IR HR AR LC DM #
LONG MESSAGE (@)LMSG(47) (CPU11)	LMSG(47) S D	Outputs a 32-character message to either a Programming Console, or a device connected via the RS-232C interface. The output message must be in ASCII beginning at address S. The destination of the message is designated in D: 000 specifies that the message is to be output to the GPC; 001 specifies the RS-232C interface, starting with the leftmost byte; and 002 specifies the RS-232C interface, starting from the rightmost byte.	S: D:: IR #000 Not HR #001 used. AR #002 LR TC DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
TERMINAL MODE (@)TERM(48) (CPU11)	TERM(48)	When the execution condition is ON, the Programming Console operation mode is changed to TERMINAL mode. There is no program command available to change the mode back to CONSOLE mode. Pressing the CHNG key on the Programming Console manually toggles between the two modes.	None
SET SYSTEM (@)SYS(49) (CPU11)	SYS(49) P	Used to either control certain operating parameters, or to execute the system commands that can be executed from the AR area.  The contents of the leftmost 8 bits (i.e., bits 08 to 15) of P determine which function SYS(49) will have. If they contain A3, then bit 00 specifies whether the battery will be checked, and bit 07 specifies whether I/O status will be maintained on start up. Bit 06 specifies whether the Force Status Hold Bit is set.  To be effective SYS(49) must be programmed at address 00001 with LD AR 1001 at address 00000. If the leftmost 8 bits of P are 00, one of seven possible System Commands, as specified by the rightmost 8 bits, will be executed (this option is not available with C200H PCs). These commands can be used to set or back-up the contents of the Parameter Area (in the DM area).	P:: # Not used.
PROGRAM PROTECT PPR(49) NTLP	PPR(49)	The user can create a unique password (P) to prevent unauthorized access to the program.	P: #
BINARY ADD (@)ADB(50)	ADB(50) Au Ad R	Adds the 4-digit augend (Au), 4-digit addend (Ad), and content of CY and outputs the result to the specified result word (R).  Au  + Ad  + CY  R  CY	Au/Ad: R: IR IR SR HR HR AR AR LR LR DM TC DM #

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand	d Data Areas
BINARY SUBTRACT (@)SBB(51)	SBB(51) Mi Su R	Subtracts the 4-digit hexadecimal subtrahend (Su) and content of carry, from the 4-digit hexadecimal minuend (Mi), and outputs the result to the specified result word (R).  Mi - Su - CY R  CY	Mi/Su: IR SR HR AR LR TC DM #	R: IR HR AR LR DM
BINARY MULTIPLY (@)MLB(52)	MLB(52) Md Mr R	Multiplies the 4-digit hexadecimal multiplicand (Md) and 4-digit multiplier (Mr), and outputs the 8-digit hexadecimal result to the specified result words (R and R+1). R and R+1 must be in the same data area.  Md  X Mr  Quotient R  Remainder R+1	Md/Mr: IR SR HR AR LR TC DM #	R: IR HR AR LR DM
BINARY DIVIDE (@)DVB(53)	DVB(53) Dd Dr R	Divides the 4-digit hexadecimal dividend (Dd) by the 4-digit divisor (Dr), and outputs result to the designated result words (R and R + 1). R and R + 1 must be in the same data area.  D  d  Dr  Quotient R  Remainder R+ 1	Dd/Dr: IR SR HR AR LR TC DM #	R: IR HR AR LR
DOUBLE BCD ADD (@)ADDL(54)	ADDL(54) Au Ad R	Adds two 8-digit values (2 words each) and the content of CY, and outputs the result to the specified result words. All words for any one operand must be in the same data area.  Au+ 1 Au  + Ad+ 1 Ad  + CY  CY R+ 1 R	Au/Ad: IR SR HR AR LR TC DM	R: IR HR AR LR DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name .	Symbol	Function	Operand Data Areas
Mnemonic  DOUBLE BCD SUBTRACT (@)SUBL(55)	SUBL(55) Mi Su R	Subtracts both the 8-digit BCD subtrahend and the content of CY from an 8-digit BCD minuend, and outputs the result to the specified result words. All words for any one operand must be in the same data area.  Mi + 1 Mi  - Su + 1 Su  - CY  R + 1 R	Mi/Su: R: IR IR SR HR HR AR AR LR LR DM TC DM
DOUBLE BCD MULTIPLY (@)MULL(56)	MULL(56)  Md  Mr  R	Multiplies the 8-digit BCD multiplicand and 8-digit BCD multiplier, and outputs the result to the specified result words. All words for any one operand must be in the same data area.  Md+ 1 Md  X Mr+ 1 Md  R+3 R+2 R+1 R	Md/Mr: R: IR IR SR HR HR AR LR DM TC DM
DOUBLE BCD DIVIDE (@)DIVL(57)	DIVL(57) Dd Dr R	Divides the 8-digit BCD dividend by an 8-digit BCD divisor, and outputs the result to the specified result words. All words for any one operand must be in the same data area.  Dd + 1 Dd  Dr + 1 Dr  Quotient R + 1 R  Remainder R + 3 R + 2	Dd/Dr: R: IR IR SR HR HR AR AR LR LR DM TC DM

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		

Name Mnemonic	Symbol	Function	Operand	d Data A	Areas
DOUBLE BCD-TO- DOUBLE BINARY (@)BINL(58)		Converts the BCD value of the two source words (S: starting word) into binary and outputs the converted data to the two result words (R: starting word). All words for any one operand must be in the same data area.	S: IR SR HR AR LR TC DM	R: IR HR AR LR DM	
DOUBLE BINARY-TO- DOUBLE BCD (@)BCDL(59)	BCDL(59) S R	Converts the binary value of the two source words (S: starting word) into eight digits of BCD data, and outputs the converted data to the two result words (R: starting result word). Both words for any one operand must be in the same data area.	S: IR SR HR AR LR DM	R: IR HR AR LR DM	
DOUBLE COMPARE (@)CMPL(60) (C200H-CPU11-E)		Compares the 8-digit hexadecimal values in words $S_1+1$ and $S_1$ with the values in $S_2+1$ and $S_2$ , and indicates the result using the Greater Than, Less Than, and Equal Flags in the AR area. $S_1+1$ and $S_2+1$ are regarded as the most significant data in each pair of words.	S <sub>1</sub> ,S <sub>2</sub> : IR SR HR AR LR TC DM		
REVERSIBLE DRUM COUNTER (@)RDM(60)	RDM(60)  N  T  R	Creates a reversible ring counter in TC 500 to TC 511 that counts from 0 to 9999, compares the PV to a table of ranges, and turns ON corresponding bits in R whenever the PV is within one of the ranges given in the table.  The size of the table is determined by the value of n, specified by bits 00 to 07 of T. The table starting at T must be within one data area, and all table words from T+1 on must be in BCD.	N: TC 500 through TC 511	IR SR HR AR LR TC	R: R: R: R: R: R: R: R: R: R: R: R: R: R
HIGH-SPEED DRUM COUNTER (C_H) HDM(61)	HDM(61) T R	Compares the PV of the high-speed counter (CNT 511) to a table of ranges, and turns ON corresponding bits in R whenever the PV is within one of the ranges given in the table. The size of the table is determined by the value of n, specified by bits 00 to 07 of T. The table starting at T must be within one data area, and all table words from T+1 on must be in BCD.	T: IR SR HR AR LR TC DM		: Not used.

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas		
HIGH-SPEED DRUM COUNTER (C_K) HDM(61)	HDM(61) NR	A 2-kHz counter with both hardware and software resets. Compares the PV of the high-speed counter (CNT 511) to a table of ranges in words DM 32 to DM 63, and turns ON corresponding bits in the result word, R, whenever the PV is within one of the ranges given in the table. Software resets may experience some delay due to the scan time. Hardware resets are independent of the the scan time and can operate at speeds of up to 2 kHz. To use the hardware reset DIP switch pins 7 and 8 must be set to ON. If the hardware reset is not being used, the DIP switches must be set to OFF.	N: R: 47 IR HR DM		
KEY INPUT (@)KEY(62)	KEY(62) S	Performs Programming Console operations from within the program. S designates the first word containing a key code. The key codes will produce the same effect as pressing the equivalent Programming Console keys.	S:: # Not used.		
END WAIT (@)ENDW(62)	——ENDW(62) N	Used to force PC to treat the specified time as the minimum scan time before beginning a new scan. If the specified time is longer than the actual scan time required, the PC will wait (after the END(01) instruction) until the specified time has elapsed. If the normal scan time exceeds the minimum time specified with ENDW(62), the scan will continue as normal.	N: IR HR TC DM #		
NOTATION INSERT (@)NETW(63)		The NETW(63) instruction is not executed. It allows the programmer to insert two hexadecimal comments within the program.	C1: # C2: #		
COLUMN-TO-WORD (@)CTW(63) (C200H-CPU11-E)	CTW(63) S C D	Fetches data from the same numbered bit (C) in 16 consecutive words (where S is the address of the first source word), and creates a 4-digit word by consecutively placing the data in the bits of the destination word, D.  The bit from word S is placed into bit 00 of D, the bit from word S+1 is placed into bit 01, etc.  Bit C D  S 0 0 0 00 S+1 1 01 S+15 0 15	S: C: D: IR IR IR SR SR SR HR HR HR AR AR AR LR LR LR TC TC TC DM DM DM #		

Data Areas: These footnote tables show the bit addresses (word addresses are given for DM and TC) of all data areas for each PC. To change bit addresses to word addresses, remove the rightmost two digits for word addresses.

	PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
CZ	_H 200H 000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Da	ata Areas
WORD-TO-COLUMN (@)WTC(64) (C200H-CPU11-E)	WTC(64) S D C	Places bit data from the source word (S), consecutively into the same numbered bits of the 16 consecutive destination words (where D is the address of the first destination word).  Bit 00 from word S is placed into bit C of word D, bit 01 from word S is placed into bit C of word D+1, etc.	S: D: IR IR SR SF HR HF AR AF LR LR TC TC DM DM	IR R SR R HR R AR LR C TC
HOURS-TO-SECONDS (@)HTS(65) (CPU11)	——————————————————————————————————————	Converts a time given in hours/minutes/ seconds (S and S+1) to an equivalent time in seconds only (R and R+1). S and S+1 must be BCD and within one data area. R and R+1 must also be within one data	S: R: IR IR SR SF HR HF AR AF	Not Rused. R
SECONDS-TO-HOURS (@)STH(66) (CPU11)	STH(66) S R	area.  Converts a time given in seconds (S and S+1) to an equivalent time in hours/minutes/seconds (R and R+1). S and S+1 must be BCD between 0 and 35,999,999, and within the same data area. R and R+1 must also be within one data area.	LR LR TC TC DM DM S: R: IR IR SR SF HR HF AR AF LR LR TC DM DM	: Not s used.
BIT COUNTER (@)BCNT(67)	BCNT(67)  N SB R	Counts the number of ON bits in one or more words (SB is the beginning source word) and outputs the result to the specified result word (R). N gives the number of words to be counted. All words in which bit are to be counted must be in the same data area.	N: R: IR IR SR HF HR AF LR TC DM DM	IR R SR R HR L AR C LR

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
BLOCK COMPARE (@)BCMP(68)	BCMP(68) S CB R	Compares a 1-word binary value (S) with the 16 ranges given in the comparison table (CB is the starting word of the comparison block). If the value falls within any of the ranges, the corresponding bits in the result word (R) will be set. The comparison block must be within one data area.	S: CB: R: IR IR IR SR SR HR HR AR LR LR LC TC TC TC DM DM DM #

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
VALUE CALCULATE (@)VCAL(69) (CPU11)	VCAL(69) C S D	Calculates the cosine, or sine of the given degree value, or determines the y-coordinate of the given x value in a previously established line graph. For the sine and cosine conversions, S is entered in BCD as an angle (in the range 0.0 to 90.0 degrees). When calculating the y-coordinate in a graph, S gives the address of the value of the x-coordinate. The calculated data is transferred to the destination word (D). Sine and cosine results are given in BCD. Line graph coordinate calculations (interpolation) can be in BCD or BIN. The data in the control word (C) determines which operation is performed. If C is entered as a constant with a value of 0000 or 0001, the sine or cosine, respectively, of the source data value is calculated. If C is entered as a word designation, it gives the address of the first word of the data table for the line graph. The value of the first two digits gives m-1, where m is the number of data points for which coordinates are given on the line graph. Bits 14 and 15, respectively, specify the output and input data formats (0 indicates BCD, 1 indicates binary).  Y  Y  X1  X2  X3  X4  X4  Xm  X  Output data format m-1, where m is the number of data points for which coordinates are given on the line graph. Bits 14 and 15, respectively, specify the output and input data formats (0 indicates BCD, 1 indicates binary).	C: S: D: IR SR SR SR HR HR AR LR TC DM DM #

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand	d Data	Areas
BLOCK TRANSFER (@)XFER(70)	XFER(70)  N S D	Moves the content of several consecutive source words (S gives the address of the starting source word) to consecutive destination words (D is the starting destination word). All source words must be in the same data area, as must all destination words. Transfers can be within one data area or between two data areas, but the source and destination words must not overlap.	N: IR SR HR AR LR TC DM #	S: IR HR AR LR TC DM	D: IR SR HR AR LR TC DM #
		$\begin{array}{c c} S & D \\ \hline S+1 & D+1 \\ \hline \end{array}$ No. of Words			
BLOCK SET (@)BSET(71)	BSET(71) S St E	Copies the content of one word or constant (S) to several consecutive words (from the starting word, St, through to the ending word, E). St and E must be in the same data area.	St/E: IR HR AR LR TC DM	S: IR SR HR AR LR TC DM #	
SQUARE ROOT (@)ROOT(72)		Computes the square root of an 8-digit BCD value (Sq and Sq + 1) and outputs the truncated 4-digit, integer result to the specified result word (R). Sq and Sq + 1 must be in the same data area.	Sq: IR SR HR AR LR TC DM	R: IR HR AR LR DM	
DATA EXCHANGE (@)XCHG(73)	XCHG(73) E1 E2	Exchanges the contents of two words (E1 and E2).	E1/E2: IR HR AR LR TC DM		

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
ONE DIGIT SHIFT LEFT (@)SLD(74)	SLD(74) St E	Shifts all data, between the starting word (St) and ending word (E), one digit (four bits) to the left, writing zero into the rightmost digit of the starting word. St and E must be in the same data area.  St St + 1	St/E: IR HR AR LR DM
ONE DIGIT SHIFT RIGHT (@)SRD(75)	SRD(75) E St	Shifts all data, between starting word (St) and ending word (E), one digit (four bits) to the right, writing zero into the leftmost digit of the ending word. St and E must be in the same data area.	St/E: IR HR AR LR DM
4-TO-16 DECODER (@)MLPX(76)	MLPX(76) S Di R	Converts up to four hexadecimal digits in the source word (S), into decimal values from 0 to 15, and turns ON the corresponding bit(s) in the result word(s) (R). There is one result word for each converted digit. Digits to be converted are designated by Di. (The rightmost digit specifies the first digit. The next digit to the left gives the number of digits to be converted minus 1. The two leftmost digits are not used.)	S: Di: R: IR IR IR SR HR HR HR AR AR AR LR LR LR TC DM TC DM DM #
16-TO-4 ENCODER (@)DMPX(77)	DMPX(77) S R Di	Determines the position of the leftmost ON bit in the source word(s) (starting word: S) and turns ON the corresponding bit(s) in the specified digit of the result word (R). One digit is used for each source word. Digits to receive the converted values are designated by Di. (The rightmost digit specifies the first digit. The next digit to left gives the number of words to be converted minus 1. The two leftmost digits are not used.)  15 00 0 to F	S: R: Di: IR IR IR SR HR HR HR AR AR AR LR LR LR DM TC TC DM DM #

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name .	Symbol	Function	Operand Data Areas
7-SEGMENT DECODER (@)SDEC(78)	SDEC(78) S Di D	Converts hexadecimal values from the source word (S) into 7-segment display data. Results are placed in consecutive half-words, starting at the first destination word (D). Di gives digit and destination details. (The rightmost digit gives the first digit to be converted. The next digit to the left gives the number of digits to be converted minus 1. If the next digit is 1, the first converted data is transferred to left half of the first destination word. If it is 0, the transfer is to the right half).	S: Di: D: IR IR IR SR HR HR HR AR AR AR LR LR TC DM TC DM DM #
FLOATING POINT DIVIDE (@)FDIV(79)	Dd Dr R	Divides one floating point value by another and outputs a floating point result. The rightmost seven digits of each set of two words (eight digits) are used for mantissa, and the leftmost digit is used for the exponent and its sign (Bits 12 to 14 give the exponent value, 0 to 7. If bit 15 is 0, the exponent is positive; if it's 1, the exponent is negative).  Dd+ 1 D  R+1 R	Dd/Dr: R: IR IR SR HR HR AR AR LR LR DM TC DM
SINGLE WORD DISTRIBUTE (@)DIST(80)	DIST(80) S DBs Of	Moves one word of source data (S) to the destination word whose address is given by the destination base word (DBs) plus offset (Of).    Base (DBs) Offset (OF)  (S) (DBs + Of)	S: DBs: Of: IR IR IR SR HR HR HR AR AR LR LR LR TC TC TC DM DM DM #

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name	Symbol	Function	Operand	Data	Areas
Mnemonic	Cymuc.		о розили		
DATA COLLECT (@)COLL(81)	COLL(81) SBs Of D	Extracts data from the source word and writes it to the destination word (D). The source word is determined by adding the offset (Of) to the address of the source base word (SBs). The offset cannot be entered as a constant when using C120 or C500 PCs.  Base (DBs)  Offset (OF)  (SBs+Of)  (D)	SBs: IR SR HR AR LR TC DM	Of: IR HR AR LR TC DM #	D: IR HR AR LR TC DM
MOVE BIT (@)MOVB(82)	MOVB(82) S Bi D	Transfers the designated bit of the source word or constant (S) to the designated bit of the destination word (D). The rightmost two digits of the bit designator (Bi) specify the source bit. The two leftmost digits specify the destination bit.	S: IR SR HR AR LR DM #	Bi: IR HR AR LR TC DM #	D: IR HR AR LR DM
MOVE DIGIT (@)MOVD(83)	MOVD(83) S Di D	Moves hexadecimal content of up to four specified 4-bit source digit(s) from the source word to the specified destination digit(s) (S gives the source word address. D specifies the destination word). Specific digits within the source and destination words are defined by the Digit Designator (Di) digits. (The rightmost digit gives the first source digit. The next digit to the left gives the number of digits to be moved. The next digit specifies the first digit in the destination word.)	S: IR SR HR AR LR TC DM #	Di: IR HR AR LR TC DM #	D: IR SR HR AR TC DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name	Symbol	Function	Operand Data Areas
Mnemonic  REVERSIBLE SHIFT REGISTER (@)SFTR(84)	SFTR(84) C St E	Shifts bits in the specified word or series of words either left or right. Starting (St) and ending words (E) must be specified. Control word (C) contains shift direction, reset input, and data input. (Bit 12: 0 = shift right, 1 = shift left. Bit 13 is the value shifted into the source data, with the bit at the opposite	St/E/C: IR HR AR TC LR DM
		end being moved to CY. Bit 14: 1 = shift enabled, 0 = shift disabled. If bit 15 is ON when SFTR(89) is executed with an ON condition, the entire shift register and CY will be set to zero.) St and E must be in the same data area and St must be less than or equal to E.	
		15 14 13 12 11 00  Not used  15 00 15 00  E St IN	
		15 00 15 00 IN E St CY	
TABLE COMPARE (@)TCMP(85)	TCMP(85) CD TB R	Compares a 4-digit hexadecimal value (CD) with values in table consisting of 16 words (TB: is the first word of the comparison table). If the value of CD falls within any of the comparison ranges, corresponding bits in result word (R) are set (1 for agreement, and 0 for disagreement). The table must be entirely within the one data area.	CD: TB/R: IR IR HR AR LR TDM DM #
		Tb+1 1 0 1 1 Tb+14 Tb+15 1 1 agreement 0: disagreement	

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand	Data Ar	reas
ASCII CONVERT (@)ASC(86)		Converts hexadecimal digits from the source word (S) into 8-bit ASCII values, starting at leftmost or rightmost half of the starting destination word (D). The rightmost digit of Di designates the first source digit. The next digit to the left gives the number of digits to be converted. The next digit specifies the whether the data is to be transferred to the rightmost (0) or leftmost (1) half of the first destination word. The leftmost digit specifies parity:  0: none, 1: even, or 2: odd.	IR SR HR AR LR	IR II HR F LR L	D: R HR -R DM
		S 0 to F D 8-bit data			
I/O WRITE (@)WRIT(87)	WRIT(87) N S D	Transfers word data through I/O word (D) allocated to a Special I/O Unit and sequentially writes data to the memory area of the I/O Unit. N is the number of words to be transferred, and S is the address of the first PC source word to be transferred. The EQ Flag is set when the transfer is completed.	IR SR HR AR LR TC		D: R
I/O READ (@)READ(88)	READ(88) N S D	READ(88) reads data from memory area of a Special I/O Unit and transfers it through word (S) allocated to the I/O Unit to destination words (D gives the address of the first destination word). N is the number of words to be transferred. The EQ Flag is set when the transfer is completed.	IR SR HR AR LR TC DM	IR II D: H IR A HR L AR T	D: R HR AR LR FC DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol		Function		Operar	nd Data /	Areas
INTERRUPT CONTROL (@)INT(89)		rupts Units fines designates to 07 higheresporthrous spon code	rols programmed (so and interrupts from a Each PC can have up the source of the intergrate the no. of the sa scheduled interrupt identify the interrupt or bits are not used. Bit onds to interrupt sigh to bit 07 of Unit ds to subroutine 31. C, the meaning of whi alue of N, as follows:	CC: N: 000 to 000 to 002	D: IR HR AR LC DM #		
		СС	N = 000 to 003	N = 004			
		000	to the data in D. Bits cor- responding to ON bits in D are masked, those cor- responding to OFF bits are unmasked. Masked bits are recorded and will	The interrupt time interval is set according to the data in D (00.01 to 99.99 s) The decimal point is not entered. The interrupt is cancelled if D is 00.00.			
		001	Unit (N) according to the corresponding ON bits in D. The subroutines corresponding to bits cleared in this manner will not be	The time to the first interrupt is set according to the data in D (00.01 to 99.99 s) The decimal point is not entered. The interrupt is cancelled if D is			
		002	Copies the mask status of the designated IIU to D.	Copies the time in- terval data to D.			

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
NETWORK SEND (@)SEND(90) (for CPUs not supporting SYSMAC LINK)	SEND(90) S D C	Sends data to a device linked via a NET Link Unit. S is the starting word of the source data to be sent from the PC. D is the starting destination word in the node into the data is to be written. C is the first of three control words. The first control word (C) gives the number of words to be transferred. In C+1, the left half designates either NSB (00) or NSU (01), and the right half gives the network number. In C+2, the left half gives the port number, and the right half gives the node number. If the destination node number is set to 0, data is sent to all nodes.  Source  Node N  S  D  D+1  C+1  NSB/NSU designation Network no. (0 to 255)  C+2  Destination port no. Destination node no. (010 127)	S: D/C: IR IR SR HR HR AR AR LR TC TC DM DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
NETWORK SEND (@)SEND(90) (C200H-CPU11-E) (for CPUs supporting SYSMAC LINK)	SEND(90) S D C	Transfers data from n source words (S is the starting word) to the destination words (D is the first address) in node N of the specified network (in a SYSMAC LINK or NET Link System). The format of the control words varies depending on the type of system. In both types of systems, the first control word (C) gives the number of words to be transferred.  For NET Link Systems, in word C+1, bit 14 specifies the system (0 for system 1, and 1 for system 0), and the rightmost 7 bits define the network number. The left half of word C+2 specifies the destination port (00: NSB, 01/02: NSU), and the right half specifies the destination node number. If the destination node number is set to 0, data is transmitted to all nodes.  For SYSMAC LINK Systems, the right half of C+1 specifies the response monitoring time (default 00: 2 s, FF: monitoring disabled), the next digit to the left gives the maximum number of re-transmissions (0 to 15) that the PC will attempt if no response signal is received. Bit 13 specifies whether a response is needed (0) or not (1), and bit 14 specifies the system number (0 for system 1, and 1 for system 0). The right half of C+2 gives the destination node number. If this is set to 0, the data will be sent to all nodes.  NET Link  C n: no. of words to be transmitted (0 to 1000)  C+1 0xx0 Re-trans Response monitor time missions (0: 110 25.4 s)  C+2 Destination port no. Destination node no. (0: 10: 126)  SYSMAC LINK  C n: no. of words to be transmitted, 0 to 1000  C+1 0xx0 Re-trans Response monitor time missions (0: 110 25.4 s)  C+2 0000 0000 Destination node no. (0: 10: 62)	S: D/C: IR IR SR HR AR AR LC TC DM DM
HIGH-SPEED PROGRAM END HEND(90)	HEND(90)	Designates the end of a high-speed program. The normal program follows. The high-speed program is executed every 10 ms, regardless of the status of the normal program execution.	None

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
SUBROUTINE ENTER (@)SBS(91)	SBS(91) N	Calls subroutine N. Moves program operation to the specified subroutine.	<b>N:</b> 00 to 99
SUBROUTINE START SBN(92)	SBN(92) N	Marks the start of subroutine N.	<b>N:</b> 00 to 99
RETURN RET(93)	RET(93)	Marks the end of a subroutine and returns control to the main program.	None
WATCHDOG TIMER REFRESH (@)WDT(94)	WDT(94) T	Sets the maximum and minimum limits for the watchdog timer (normally 0 to 130 ms). New limits: Maximum time = $130 + (100 \times T)$ Minimum time = $130 + (100 \times (T-1))$	T: 0 to 63
BLOCK PROGRAM START BPRG(96)	BPRG(96) N	Indicates the beginning of a block program. Block programs allow flowchart-style programming within ladder diagram programs.	<b>N:</b> 00 to 99
I/O REFRESH (@)IORF(97)	IORF(97)   St   E	Refreshes all I/O words between the start (St) and end (E) words. Only I/O words may be designated. Normally these words are refreshed only once per scan, but refreshing words before use in an instruction can increase execution speed. St must be less than or equal to E.	St/E: IR

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
NETWORK RECEIVE (@)RECV(98) (for CPUs not supporting SYSMAC LINK)	RECV(98) S D C	Receives data from a device linked through a NET Link Unit. S is the starting source word in the node from which the data is to be read; D is the starting destination word in PC to receive the data; C is the address of the first of three control words. The first control word gives the number of words to be transferred. In the second control word, the left half designates the NSB (0) or NSU (1), and the right half specifies the network number. In the third word, the left half specifies the port number, and the right half, the node number.  Source node N Destination node  S D  S+1 D+1  C n: no. of words to be transmitted (0 to 1000)  C+1 NSB/NSU designation Network no. (010 255)  C+2 Source port no. Source node no. (010 127)	S: D/C: IR IR SR HR HR AR AR LR LR TC TC DM DM

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

Name	Symbol			Function	n e	Opera	nd Data Areas
Mnemonic	Symbol			i uncu	JII	Opera	nu Data Aleas
NETWORK RECEIVE (@)RECV(98) (C200H-CPU11-E) (for CPUs supporting SYSMAC LINK)	RECV(98) S D C	the first netwo Syster at D. Tries do both it word (transfe For NE (C+1), syster rightm ber. The source the rightm to 15) spons wheth (1), ar ber (0 The rightm ode it in ode it	st word) firk (in a Sm) to the The formal epending ypes of C) gives erred. ET Link Sm 1, and ost 7 bits he left half sport (00 of the new num num that the esignal if er a respending he sport (14 for systems) and bit 14 for systems of with the systems of the sys	om node YSMAC destinate at of the on the systems, pecifies 1 for sistence of the following state of the systems	source words (S is a N of the specified LINK or NET Link ion words starting control words vatype of system. In s, the first control iber of words to be in the second word the system (0 for ystem 0), and the the network number of C+2 specifies the 01/02: NSU), and the source node tems, the right half sponse monitoring is the left gives the extransmissions (0 attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies needed (0) or not attempt if no read. Bit 13 specifies	S: IR SR HR AR LTC DM	C/D: IR HR AR LR TC DM

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
HIGH-SPEED DRUM COUNTER (C_P) HDM(98)	——————————————————————————————————————	A 2-kHz counter with both hardware and software resets. Compares the PV of the high-speed counter (CNT 511) to a table of ranges in words DM 32 to DM 63, and turns ON corresponding bits in the result word, R, whenever the PV is within one of the ranges given in the table. Software resets may experience some delay due to the scan time. Hardware resets are independent of the the scan time and can operate at speeds of up to 2 kHz. To use the hardware reset DIP switch pins 7 and 8 must be set to ON. If the hardware reset is not being used, the DIP switches must be set to OFF.	• • • • • • • • • • • • • • • • • • • •
RUN STOP STOP(99)	—— STOP(99)	Stops the RUN operation when the execution condition is OFF, and starts operation when ON.	None

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		

## 4-3 Block Program Instructions

Name Mnemonic	Symbol	Function	Operand Data Areas
BLOCK PROGRAM END BEND<01>	BEND<01>	Indicates the end of a block program.	None
CONDITIONAL BRANCH IF<02> IF<02> B IF<02> NOT B	IF<02> IF<02> NOT	Indicates the part of the program that is to be executed when a given condition is satisfied.	B: IR SR HR AR LR TC
NO BRANCH ELSE<03>	ELSE<03>	Specifies the part of the program that is to be executed when the IF condition is not satisfied.	None
BRANCH END IEND<04>	IEND<04>	Defines the end of the program portion that has started with IF<02>.	None
ONE SCAN AND WAIT WAIT<05> WAIT<05> B WAIT<05> NOT B	WAIT<05> WAIT<05> NOT	Halts execution of a block program until a specified condition is satisfied.	B: IR SR HR AR LR TC
CONDITIONAL BLOCK EXIT EXIT<06> EXIT<06 B EXIT<06> NOT B	EXIT<06> EXIT<06> NOT	Exits a block program if a given condition is satisfied.	B: IR SR HR AR LR TC
SET SET<07> B	SET<07>	Sets (turns ON) the specified bit.	B: IR HR AR LR
RESET RSET<08> B	RSET<08>	Resets (turns OFF) the specified bit.	B: IR HR AR LR
LOOP LOOP<09>	LOOP<09>	Defines the beginning of section to be repeated until a specified terminal condition is satisfied.	None
LOOP END LEND<10> LEND<10> B LEND<10> NOT B	LEND<10> LEND<10> NOT	Defines the end of the section to be repeated. Execution of the specified section continues until the terminal condition is satisfied.	B: IR SR HR AR LR TC
BLOCK PROGRAM PAUSE BPPS<11> N	BPPS<11>	Causes the execution of designated block program to pause until a specified condition is satisfied (often used in conjunction with a timer or counter).	<b>N</b> : 0 to 99

PC	IR	SR	HR	TR	AR	LR	TC	DM	Constants (#)
C500/C120	0000 to 6002	6003 to 6307	HR 0000 to 3115	TR 0 to 7	None	LR 000 to 3115	TC 000 to 127	DM 000 to DM 511	0000 to 9999 or 0000 to FFFF
C20/C_K/ C_P	0000 to 1807	1808 to 1907	HR 000 to 915	TR 0 to 7	None	None	TC 00 to 47	DM 00 to DM 63 (C20: no DM area)	0000 to 9999 or 0000 to FFFF

Name Mnemonic	Symbol	Function	Operand Data Areas
BLOCK PROGRAM RESTART BPRS<12> N	BPRS<12>	Restarts execution of the designated block program.	<b>N</b> : 0 to 99
TIMER WAIT TIMW<13> N SV	TIMW<13>	The execution of the block program between the TIMW<13> instruction and BEND<04> is not executed until the set value of the specified timer has been reached. SV: 000.0 to 999.9.	SV: N: IR TC AR DM HR LR
COUNTER WAIT CNTW<14> N SV I	CNTW<14>	The portion of block program between the CNTW<14> instruction and BEND<04> is not executed until the set value of the specified counter has been reached.	SV: N: IR TC AR DM HR LR
HIGH-SPEED TIMER WAIT TMHW<15> N SV	TMHW<15>	The portion of program between the TIMH<15> instruction and BEND<04> is not executed until the set value of the high-speed timer has been reached. SV: 00.02 to 99.99	SV: N: IR TC AR DM HR LR

PC	IR	SR	HR	TR	AR	LR	тс	DM	Constants (#)
C_H C200H C1000H/C2000H	00000 to 24615	24700 to 25515	HR 0000 to 9915	TR 0 to 7	AR 0000 to 2715	LR 0000 to 6315	TC 000 to 511		0000 to 9999 or 0000 to FFFF

## Appendix A Programming Console Key Codes

The following codes can be used in KEY(62) to execute Programming Console operations from the user program. Refer to *Section 4 Ladder Programming* for programming details and to *Section 2 Program Programming Console Operations* for details on how they are used to input the different operations.

The keys shown below are activated with the hexadecimal code given with it. The Programming Console display can be reset to the password display by input  $\mathbf{40}_{\text{hex}}$ .

3D	3C	3B	38	39	3A
FUN	SFT	NOT	None	None	SHIFT
35	34 OR -II <sup>5</sup>	33 CNT	30 TR	31	32 HR
2D	2C out -O+	2B TIM	28 DM	29 	2A CONT #
25 7	8	9	20 EXT	21	22 SRCH
1D	1C	1B 6	18 PLAY SET	19	1A MONTR
15 B 1	14 © 2	13 D 3	10 REC RESET	11 INS	12
0D <sup>A</sup> 0	<b>0C</b> None	OB CLR	08 VER	09	0A <b>★</b>

## **Appendix B Instruction Groups**

This Appendix lists the programming instructions according to the type of operations they perform. The groupings are similar to those found in the tables of contents at the beginning of most manuals. For details on applicable PCs, see the alphanumeric listing in *Section 3. Section 4* gives a detailed description of the instruction, how it is used, its ladder symbol, and the data areas used for the operands.

### **Data Manipulation Instructions**

Mnemonic	Code	Name	Mnemonic	Code	Name
SFT	10	SHIFT REGISTER	SUBL	55	DOUBLE BCD SUBTRACT
WSFT	16	WORD SHIFT	MULL	56	DOUBLE BCD MULTIPLY
RWS	17	REVERSIBLE WORD SHIFT	DIVL	57	DOUBLE BCD DIVIDE
MCMP	19	MULTI-WORD COMPARE	BINL	58	DOUBLE BCD-TO-DOUBLE BINARY
CMP	20	COMPARE	BCDL	59	DOUBLE BINARY-TO-DOUBLE BCD
MOV	21	MOVE	CMPL	60	DOUBLE COMPARE
MVN	22	MOVE NOT	CTW	63	COLUMN-TO-WORD
BIN	23	BCD-TO-BINARY	WTC	64	WORD-TO-COLUMN
BCD	24	BINARY-TO-BCD	HTS	65	HOURS-TO-SECONDS
ASL	25	ARITHMETIC SHIFT LEFT	STH	66	SECONDS-TO-HOURS
ASR	26	ARITHMETIC SHIFT RIGHT	BCNT	67	BIT COUNTER
ROL	27	ROTATE LEFT	ВСМР	68	BLOCK COMPARE
ROR	28	ROTATE RIGHT	VCAL	69	VALUE CALCULATE
COM	29	COMPLEMENT	XFER	70	BLOCK TRANSFER
ADD	30	BCD ADD	BSET	71	BLOCK SET
SUB	31	BCD SUBTRACT	ROOT	72	SQUARE ROOT
MUL	32	BCD MULTIPLY	XCHG	73	DATA EXCHANGE
DIV	33	BCD DIVIDE	SLD	74	ONE DIGIT SHIFT LEFT
ANDW	34	LOGICAL AND	SRD	75	ONE DIGIT SHIFT RIGHT
ORW	35	LOGICAL OR	MLPX	76	4-TO-16 DECODER
XORW	36	EXCLUSIVE OR	DMPX	77	16-TO-4 ENCODER
XNRW	37	EXCLUSIVE NOR	SDEC	78	7-SEGMENT DECODER
INC	38	INCREMENT	FDIV	79	FLOATING POINT DIVIDE
DEC	39	DECREMENT	DIST	80	SINGLE WORD DISTRIBUTE
STC	40	SET CARRY	COLL	81	DATA COLLECT
CLC	41	CLEAR CARRY	MOVB	82	MOVE BIT
ADB	50	BINARY ADD	MOVD	83	MOVE DIGIT
SBB	51	BINARY SUBTRACT	SFTR	84	REVERSIBLE SHIFT REGISTER
MLB	52	BINARY MULTIPLY	TCMP	85	TABLE COMPARE
DVB	53	BINARY DIVIDE	ASC	86	ASCII CONVERT
ADDL	54	DOUBLE BCD ADD			

### **Subroutine Instructions**

Mnemonic	Code	Name	Mnemonic	Code	Name
INT	89	INTERRUPT CONTROL	SBN	92	SUBROUTINE START
SBS	91	SUBROUTINE ENTER	RET	93	RETURN

Instruction Groups Appendix B

## **Basic Instructions**

Mnemonic	Code	Name	Mnemonic	Code	Name
AND		AND	END	01	END
AND LD		AND LOAD	IL	02	INTERLOCK
AND NOT		AND NOT	ILC	03	INTERLOCK CLEAR
CNT		COUNTER	JMP	04	JUMP
LD		LOAD	JME	05	JUMP END
LD NOT		LOAD NOT	KEEP	11	KEEP
OR		OR	CNTR	12	REVERSIBLE COUNTER
OR LD		OR LOAD	DIFU	13	DIFFERENTIATE UP
OR NOT		OR NOT	DIFD	14	DIFFERENTIATE DOWN
OUT		OUTPUT	TIMH	15	HIGH-SPEED TIMER
OUT NOT		OUTPUT NOT	RDM	60	REVERSIBLE DRUM COUNTER
T∣M		TIMER	HDM	61	HIGH-SPEED DRUM COUNTER
NOP	00	NO OPERATION	HDM	98	HIGH-SPEED DRUM COUNTER

## **Special Instructions**

Mnemonic	Code	Name	Mnemonic	Code	Name
FAL	06	FAILURE ALARM	SYS	49	SET SYSTEM
FALS	07	SEVERE FAILURE ALARM	KEY	62	KEY INPUT
SCAN	18	SCAN TIME	ENDW	62	END WAIT
FILR	42	FILE MEMORY READ	NETW	63	NOTATION INSERT
FILW	43	FILE MEMORY WRITE	WRIT	87	I/O WRITE
FILP	44	EXTERNAL PROGRAM READ	READ	88	I/O READ
TRSM	45	TRACE MEMORY SAMPLE	SEND	90	NETWORK SEND
MSG	46	DISPLAY MESSAGE	WDT	94	WATCHDOG TIMER REFRESH
LMSG	47	LONG MESSAGE	IORF	97	I/O REFRESH
TERM	48	TERMINAL MODE	RECV	98	NETWORK RECEIVE
PPR	49	PROGRAM PROTECT	STOP	99	RUN STOP

## **Step and Block Instructions**

Mnemonic	Code	Name	Mnemonic	Code	Name
STEP	08	STEP DEFINE	SET	<07>	SET
SNXT	09	STEP START	RSET	<08>	RESET
BPRG	96	BLOCK PROGRAM START	LOOP	<09>	LOOP
BEND	<01>	BLOCK PROGRAM END	LEND	<10>	LOOP END
IF	<02>	CONDITIONAL BRANCH	BPPS	<11>	BLOCK PROGRAM PAUSE
ELSE	<03>	NO BRANCH	BPRS	<12>	BLOCK PROGRAM RESTART
IEND	<04>	BRANCH END	TIMW	<13>	TIMER WAIT
WAIT	<05>	ONE SCAN AND WAIT	CNTW	<14>	COUNTER WAIT
EXIT	<06>	CONDITIONAL BLOCK EXIT	TMHW	<15>	HIGH-SPEED TIMER WAIT

# Appendix C Extended ASCII ASCII Codes

Bits	0 to 3							Bits 4	4 to 7						
BIN		0000	0001	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
	HEX	0	1	2	3	4	5	6	7	Α	В	С	D	Е	F
0000	0	NUL	DLE	Space	0	@	P	۲	p		0	@	P	•	p
0001	1	SOH	DC <sub>1</sub>	!	1	A	Q	a	q	!	1	A	Q	a	q
0010	2	STX	DC <sub>2</sub>	,,	2	В	R	b	r	"	2	В	R	b	r
0011	3	ETX	DC <sub>3</sub>	#	3	С	S	c	s	#	3	С	S	c	S
0100	4	EOT	DC <sub>4</sub>	\$	4	D	T	d	t	\$	4	D	T	d	t
0101	5	ENQ	NAK	%	5	Е	U	e	u	%	5	E	U	e	и
0110	6	ACK	SYN	&	6	F	V	f	v	&	6	F	V	f	v
0111	7	BEL	ETB	,	7	G	W	g	w	,	7	G	W	g	w
1000	8	BS	CAN	(	8	Н	X	h	X	(	8	Н	X	h	x
1001	9	HT	EM	)	9	I	Y	i	y	)	9	I	Y	i	y
1010	Α	LF	SUB	*	:	J	Z	j	z	*	:	J	Z	j	z
1011	В	VT	ESC	+	;	K	[	k	{	+	;	K	[	k	{
1100	С	FF	FS	,	<	L	\	1		,	<	L	1	l	
1101	D	CR	GS	-	=	M	]	m	}	-	=	M	]	m	}
1110	Е	S0	RS	•	>	N	^	n	«	•	>	N	^	n	
1111	F	S1	US	/	?	0	_	О	~	/	?	0	_	0	~

## Appendix D Data Conversion Table

Decimal	BCD	Hexadecimal	Binary
00	00000000	00	00000000
01	0000001	01	00000001
02	0000010	02	00000010
03	00000011	03	00000011
04	00000100	04	00000100
05	00000101	05	00000101
06	00000110	06	00000110
07	00000111	07	00000111
08	00001000	08	00001000
09	00001001	09	00001001
10	00010000	0A	00001010
11	00010001	0B	00001011
12	00010010	0C	00001100
13	00010011	0D	00001101
14	00010100	0E	00001110
15	00010101	0F	00001111
16	00010110	10	00010000
17	00010111	11	00010001
18	00011000	12	00010010
19	00011001	13	00010011
20	00100000	14	00010100
21	00100001	15	00010101
22	00100010	16	00010110
23	00100011	17	00010111
24	00100100	18	00011000
25	00100101	19	00011001
26	00100110	1A	00011010
27	00100111	1B	00011011
28	00101000	1C	00011100
29	00101001	1D	00011101
30	00110000	1E	00011110
31	00110001	1F	00011111
32	00110010	20	00100000

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### **Revision History**

## SYSMAC C-series PCs Programming Instructions and Programming Console Operations

#### Reference Manual

A manual revision code appears as a suffix to the catalog number on the front cover of the manual.

The following table outlines the changes made to the manual during each revision. Page numbers refer to the previous version.

Revision code	Date	Revised content
1	September 1990	Original production
1A	January 1993	Page 2: The applicable PCs list for Buzzer ON/OFF, I/O Table Transfer, and NET LINK Table Transfer has been corrected.
		Page 22: C200H has been deleted from the applicable PCs list for Function Code 60.
		Pages 39, 41, 53, and 56: CPU11 has been clarified to C200H-CPU11-E for DOUBLE COMPARE, COLUMN-TO-WORD, WORD-TO-COLUMN, NET-WORK WRITE, and NETWORK RECEIVE.