OMRON USER'S MANUAL

Programmable Controller

Model SYSMAC-M1R

ONICS CO.

INTRODUCTION

"OMRON SYSMAC" is the trade name of OMRON's programmable controllers unparalleled in reliability and versatility.
Programmable controllers, which were initially developed to meet the demands by equipment manufacturing industries and large-scale plants for their production facilities, now answer the needs of industries from every field and have become original equipment for installation at factories.
The above trend has induced original equipment manufacturers to design the incorporation of programmable controllers in their machinery and equipment, and thus the demand for availability of the programmable controllers that can be handled as easily as components has been increasing. Accordingly, OMRON has sought to develop programmable controllers which are: a. small and economical, b. easy to handle by merely connecting a load and power and c. easy to operate by anyone at site, in addition to possessing flexibility that permits adapting to changes to the controlled systems or control parameters with simple keyboard operation and high reliability which can be materialized only by electronic control.
OMRON now offers with confidence the OMRON SYSMAC-M1R Module Type Programmable Controller, a first-class programmable controller with "CPU function" and "techniques responding adequately to the needs at every site." Programming with the SYSMAC-M1R can be performed easily and directly from ladder diagrams using the program console incorporated in the programmable controller or the optional graphic program console (CRT).
Since the programmable controller adopts the building block system, the I/O units to which controlled devices are connected, can be expanded to a maximum of 512 points in increments of 32 I/O points per unit.

CONTENTS

NOTE: For detailed information on the graphic programming console (CRT) Type SCY-CRT10-81E (-82E), please refer to the "USER'S MANUAL (Cat. No. W50-E1) for OMRON Graphic Programming Console Model SYSMAC-CRT10" published under separate cover.

1. Features

- **Conversational programming with optional graphic program console (CRT).**
  - Programming and debugging can be greatly simplified through communications between the SYSMAC-M1R and operator in a dialog mode via messages on the CRT screen.
  - The CRT console can also be used as a stand-alone since the console has its own CPU which can operate independently of the main CPU in the SYSMAC-M1R.
  - Programming time can be reduced greatly since the CRT console permits preprogramming of standardized circuits into memory, in addition to its capability to automatically display N.O. contacts which account for 60 to 70% of all ladder diagram symbols used in sequence circuits.
    Monitor function allows at-a-glance identification of relay coil ON/OFF state of a circuit to facilitate program simulation and maintenance. The CRT console also has a labelling function to facilitate the identification of I/O devices during monitoring.
- **Easy-to-use configuration**
  In addition to the program console integrated into the CPU rack, PROM writer function, cassette interface function and CRT interface function (for the CPU with CRT I/F card only) are provided as standard equipment.
- **Programs can be recorded on cassette tape**
  By connection of the exclusive interface cords, programs in the CPU memory may be dumped onto a commercially available cassette tape.
- **Instructions for sophisticated programming**
  Such instructions as ADD(+), SUB (–), MOV (I/O data transfer), CMP (I/O data compare), FAL (Diagnosis), etc. are added to facilitate sophisticated programming.
- **I/O expansion possible up to 512 points**
  The number of I/O points can be expanded up to 512 points with D I/O units alone mounted on the CPU rack and one expansion I/O rack, and 320 points with C I/O units alone mounted on the CPU rack and 4 expansion I/O racks. D I/O and C I/O units may be mixed on the CPU and expansion I/O racks.
- **High-speed counter unit, A/D conversion unit and D/A conversion unit are available as special I/O units.**
  - The high-speed counter unit is a special I/O unit capable of counting high-speed input signals and consists of a reversible counter with 6-digit BCD output and count presetters and comparators both in two stages.
  - The A/D conversion unit is a special I/O unit which has two analog input channels. For signal levels, either a voltage input of +1 to +5V or a current input of 4 to 20mA is selectable.
  - The D/A conversion unit is a special I/O unit which has two analog output channels. For signal levels, either a voltage output of +1 to +5V or a current output of 4 to 20mA is selectable.
- **Abundance of monitor and diagnostic functions for improved maintenability and operability**
  - Multi-point monitoring feature (which allows simultaneous display of 4 I/O points) facilitates delicate timing check of sequence circuits.
  - Monitoring capability such as trace (continuity) check, I/O states display, present value indication of each timer/counter, etc. assures easy program simulation and maintenance.
  - A variety of diagnostic functions provide positive system backup. All programming mistakes and operational errors are alerted immediately by electronic buzzer.

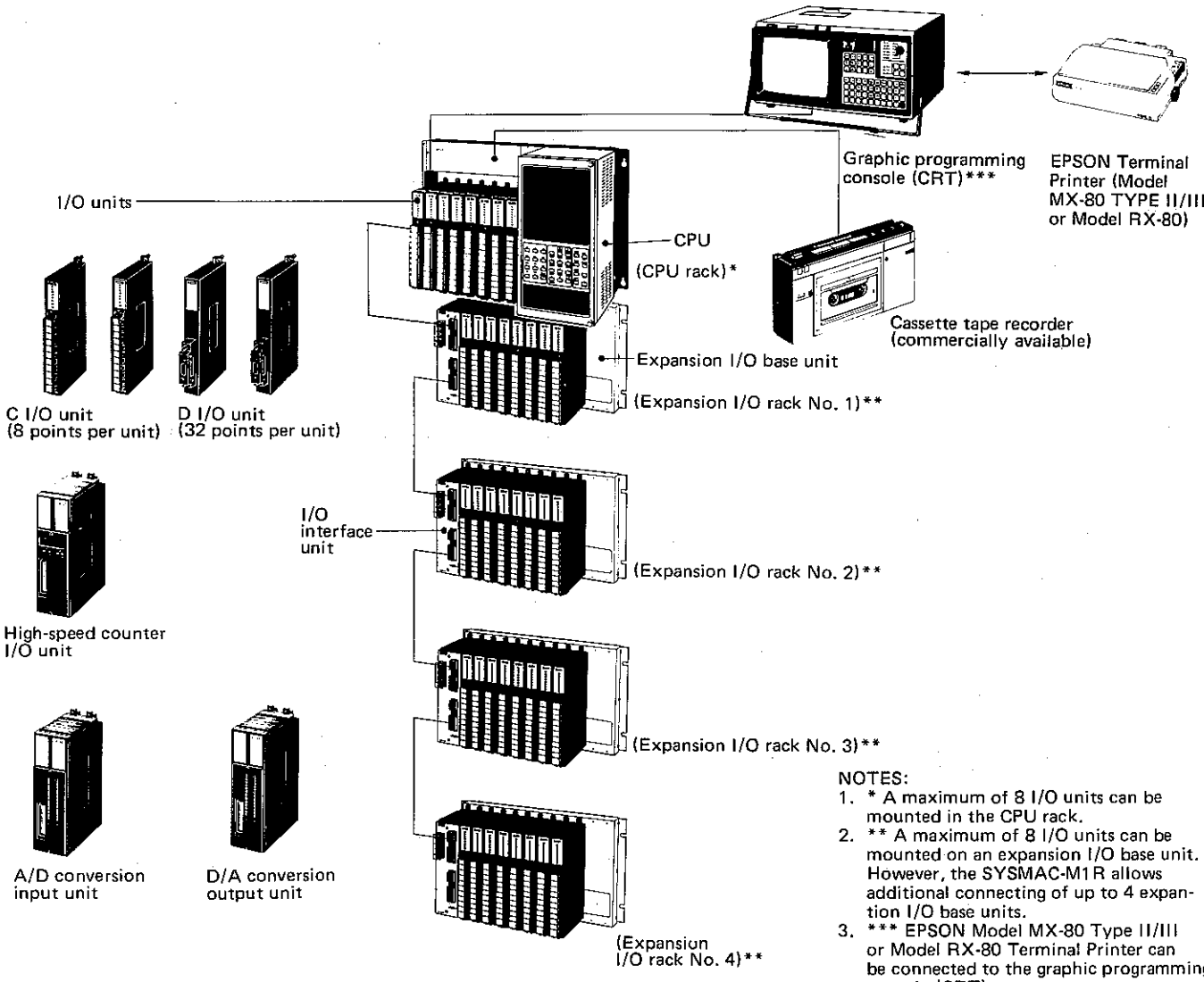
2. System Configuration and Specifications

2.1 Available Types

The SYSMAC-M1R consists of a CPU (Central Processing Unit) and input/output units. A graphic programming console is available as an optional programming support tool.

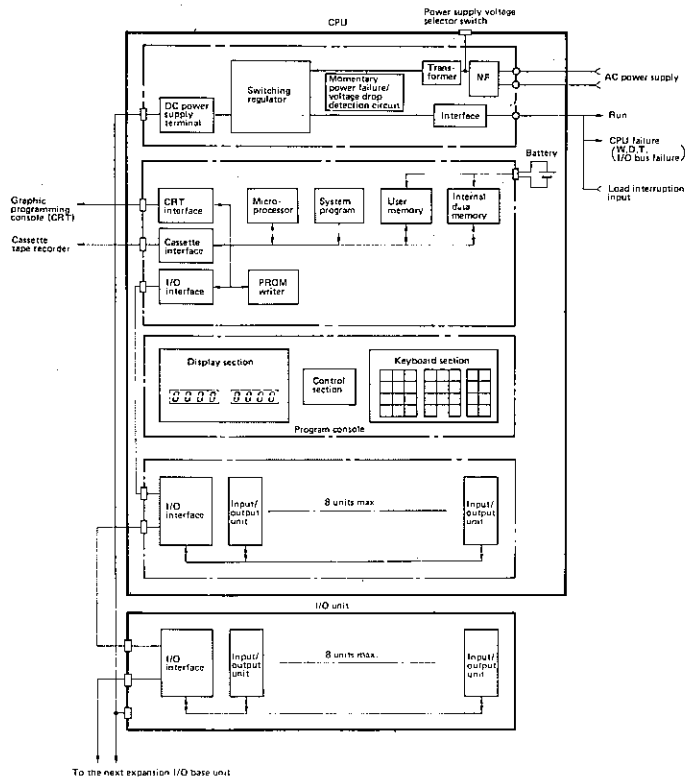
Classification			Specification	Weight	Type
CPU rack		ROM/RAM type (with PROM writer function)	Memory: 4k words (without EPROM or RAM chips) with CRT I/F card	11kg max.	SCYM1R-CPU86E
Expansion I/O rack		Expansion I/O base unit	A maximum of 8 I/O units can be mounted	2.5kg max.	SCYM1-BE122
		I/O interface unit	–	470g max.	SCYM1-IOIF1
		I/O connecting cable	Cable length: 40cm	280g max.	SCY-CN040
			Cable length: 70cm	370g max.	SCY-CN070
I/O unit	Control I/O (C I/O) unit	Input unit	DC 12V max.	220g max.	SCYM1-ID011
			DC 24V +10%, –15%		SCYM1-ID022
			AC 100/110V +10%, –15%	280g max.	SCYM1-IA101
			AC 200V +10%, –15%		SCYM1-IA201
		Output unit	Transistor output: DC 52.8V, 500mA	260g max.	SCYM1-OD041
			Triac output: AC 100 to 200V, 1A max.	352g max.	SCYM1-OA201
			Relay contact output: AC 250V, DC 24V, 2A max.	370g max.	SCYM1-OC203
	Data I/O (D I/O) unit	Input unit	DC 24V +10%, –15%	300g max.	SCYM1-DI021
		Output unit	DC 24V +10%, –15%, 100mA/point	300g max.	SCYM1-DO021
	High-speed counter I/O unit		BCD 6-digit, reversible, 10kcps max.	670g max.	SCYM1R-CNT20
	A/D conversion input unit		Input range: +1 to +5V or 4 to 20mA	770g max.	SCYM1R-AD122
	D/A conversion output unit		Output range: +1 to +5V/4 to 20mA	680g max.	SCYM1R-DA122
Peripheral equipment		Graphic programming console (CRT)	Supply voltage: AC 110/120V	13kg max.	SCY-CRT10-81E
			Supply voltage: AC 220/240V		SCY-CRT10-82E
		CRT console interface cable	Cable length: 2m (for connection between SYSMAC-M1R and SYSMAC-CRT10)	220g max.	SCY-CN200
		Cassette interface cable	Cable length: 2m (for connection between SYSMAC-M1R/ SYSMAC-CRT10 and cassette tape recorder)	50g max.	SCYP0R-PLG01
		RS-232C interface cable	Cable length: 2m (for connection between SYSMAC-CRT10 and EPSON terminal printer)	220g max.	SCY-CN201
Battery			Lithium battery	20g max.	SCYM1R-BAT80
EPROM chip*			1k words/chip	10g max.	ROM-F
RAM chip*					RAM-F

NOTES: 1. * The SYSMAC-M1R can use a maximum 4k words for programming. In this case, however 4 EPROM or RAM chips are required.
2. For detailed information on the graphic programming console (CRT) Type SCY-CRT10-81E (-82E), please refer to the "USER'S MANUAL (Cat. No. W50-E1) for OMRON Graphic Programming Console Model SYSMAC-CRT10" published under separate cover.



NOTES:
1. * A maximum of 8 I/O units can be mounted in the CPU rack.
2. ** A maximum of 8 I/O units can be mounted on an expansion I/O base unit. However, the SYSMAC-M1R allows additional connecting of up to 4 expansion I/O base units.
3. *** EPSON Model MX-80 Type II/III or Model RX-80 Terminal Printer can be connected to the graphic programming console (CRT).

2.2 System Configuration



2.3 Specifications

■ RATINGS

Supply voltage	AC 110, 120, 220 or 240V, 50/60Hz*
Operating voltage range	85 to 110% of rated voltage**
Power consumption	110VA max.
Insulation resistance	20MΩ min. at DC 500V (between external terminal and outer casing)
Dielectric strength	AC 1,500V, 50/60Hz for 1 minute (between external terminal and outer casing)
Noise immunity	1,000Vp-p Rise time: 1nsec; Pulse width: 2μsec
Vibration	16.7Hz, 3mm double amplitude, (in X, Y, Z directions, respectively 2 hrs.)
Shock	10G's (in X, Y, Z directions, respectively 3 times)
Ambient temperature	Operating: 0 to +50°C Storage: −10°C to +70°C
Humidity	30 to 90% RH (without condensation)
Atmosphere	Must be free from corrosive gases
Structure	Module type
Coating	CPU: Ivory white I/O unit: Black
Weight	See Section 2.1, Available Types.

NOTES: * Set the supply voltage selector switch to select the required voltage.

** A momentary power failure of less than 1 cycle is ignored by the programmable controller. If a momentary power failure of 1 to 2 cycle occurs, the power failure condition may or may not be detected by the programmable controller since it is in an unstable area. If a power failure of more than 2 cycle occurs, the programmable controller detects the power failure.

■ CHARACTERISTICS

Control system	Stored program system
Main control element	LSI, TTL, C-MOS
Programming system	Ladder diagram
Instruction word length	1 word or 2 words (16 bits/word)
Number of instructions	26 kinds
Execution time/word	Average: 15μsec/word
Programming capacity	RAM: 4k words EPROM: 4k words
Number of input/output points	512 points (Relay Nos. 0000 ~ 0777)
Number of internal auxiliary relays	224 points (Relay Nos. 1000 ~ 1337)
Number of special auxiliary relays	28 points (Relay Nos. 1340 to 1367, 1374 to 1377) • Relay Nos. 1340 to 1347: Output area when FAL instruction is executed. • Relay Nos. 1350 to 1357, 1360: Result area when ADD/SUB instruction is executed. • Relay Nos. 1361 to 1363: Result area when CMP instruction is executed. • Relay Nos. 1364, 1366: Normally OFF • Relay Nos. 1365, 1367: Normally ON • Relay No. 1374: Turns ON when the battery is abnormal. • Relay No. 1375: 0.2 sec clock pulse • Relay No. 1376: 1 sec clock pulse • Relay No. 1377: 0.1 sec clock pulse
Number of latching relays	256 points (Relay Nos. 000 to 377)
Number of timers and counters	128 points (Relay Nos. 000 to 177) Timer: 0 to 99.9 sec Counter: 0 to 999 counts
Number of shift registers	256 points (Relay Nos. 000 to 377) 8 bits x 32
Number of temporary memory relays	8 points (Relay Nos. 0 to 7)
Memory protective function against power failure	Status data of respective latching relays, counters and shift registers before the power failure are retained in the memory.
Diagnostic functions	■ RUN mode CPU failure (Watchdog timer) Battery failure (Rated voltage check) I/O bus failure (I/O bus diagnosis)
	■ PROGRAM mode (Program check) • Coil duplication check • END instruction check • Circuit error check (syntax check) • IL/JMP error check • Program over check

■ DIAGNOSTIC FUNCTIONS

As the diagnostic functions of the SYSMAC-M1R, checks on the items listed in the following tables are performed in the PROGRAM and RUN modes, respectively.

- **PROGRAM mode**

Diagnostic function		Function	Error indication
Item	Title		
Program check.	Coil duplication check	Checks coil numbers for duplication.	ON
	END instruction check	Checks the presence of END instruction at the end of the program	
	Circuit error check	Checks the circuit for proper configuration.	
	IL/JMP error check	Checks if IL-ILC, JMP-JME instructions are being used in pairs.	
	Program over check	Checks if the number of program steps exceeds the memory capacity in Program write or Contact (coil) addition operation.	

- **RUN mode**

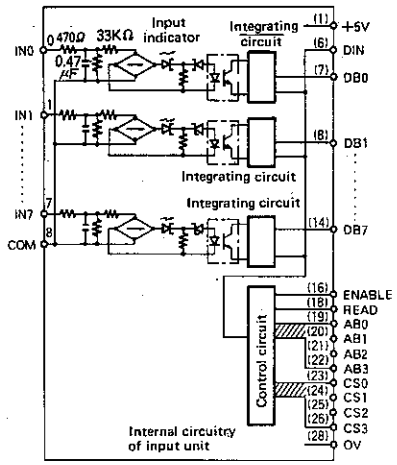
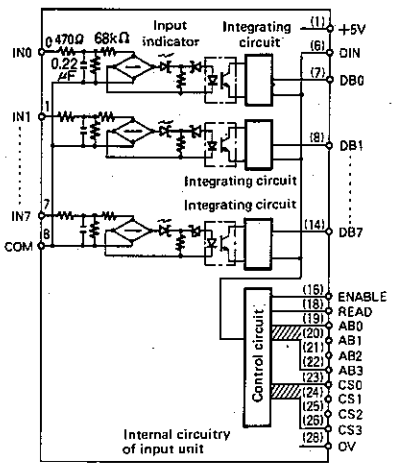
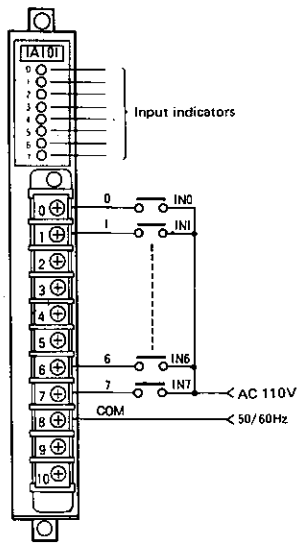
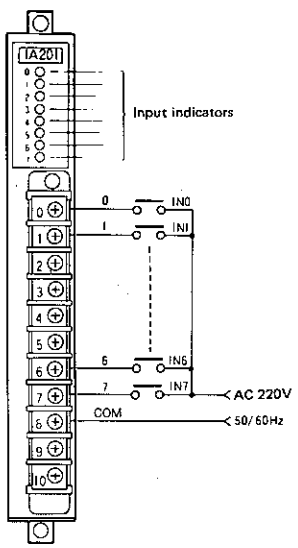
Diagnostic function		Display			Externally operated I/O relay contact** (Switching capacity 10mA to 2A)		Special internal auxiliary relay (Relay No. 1374)
Item	Title	ADDRESS	DATA	ERROR indicator	RUN output	CPU failure output	
Battery failure*	Rated voltage check	–	–	ON	–	–	ON
CPU failure	Watchdog timer				OFF	ON	–
I/O bus failure	I/O bus diagnosis						

NOTES: * If the battery is left alone for a week or more without being replaced after the ERROR indicator illuminates, the contents of the program memory will be destroyed. When the battery is to be replaced, be sure to replace it within approx. 5 minutes after turning off the power switch.

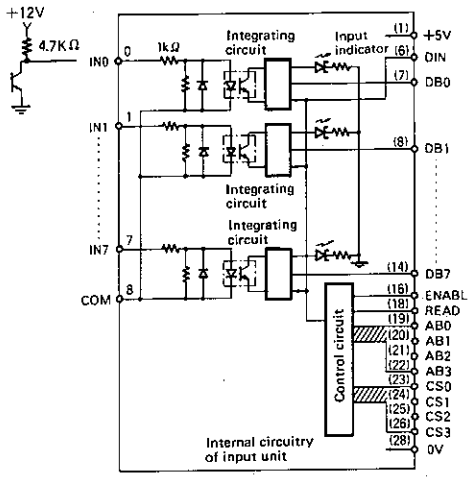
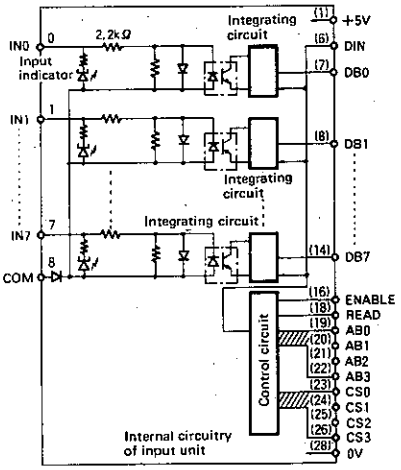
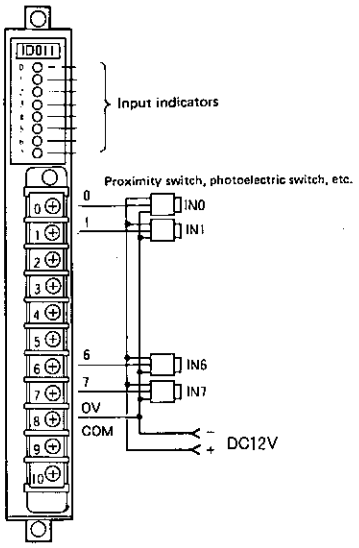
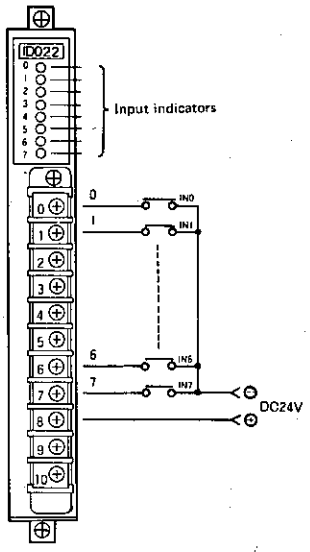
** Refer to "8.7 Hints on Use of the externally operated I/O relays."

■ CONTROL I/O (C I/O) UNITS

• Input units

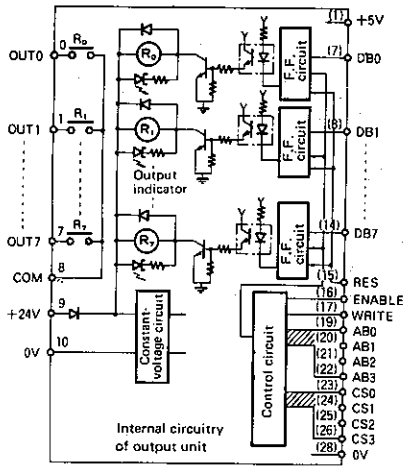
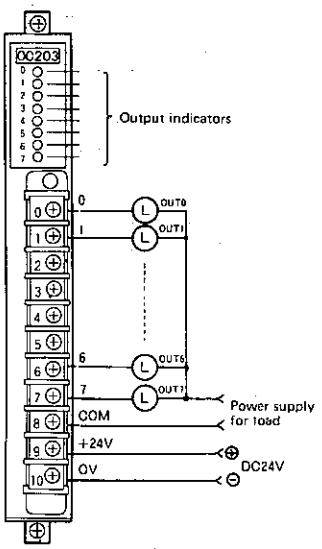
Item \ Type	AC input unit	
	Type SCYM1-IA101	Type SCYM1-IA201
Input voltage	AC 110V +10%, –15%, 50/60Hz	AC 220V +10%, –15%, 50/60Hz
Input impedance	Approx. 7kΩ	Approx. 15kΩ
Input current	16.5mA/point ±10%, 50Hz (at 110V) 19.8mA/point ±10%, 60Hz (at 110V)	16.5mA/point ±10%, 50Hz (at 220V) 19.8mA/point ±10%, 60Hz (at 220V)
ON delay time*	5 to 15msec. (Typ. 10msec.)	5 to 15msec. (Typ. 10msec.)
OFF delay time**	15 to 35msec. (Typ. 25msec.)	15 to 35msec. (Typ. 25msec.)
Number of circuits	8	8
Weight	280g ±5%	280g ±5%
OFF voltage	20V min.	40V min.
Internal circuit		
Terminal connections		

NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of the input signal until the inactivation of the output terminal of the unit.

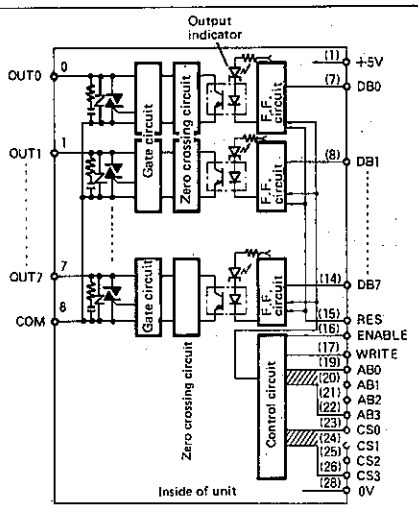
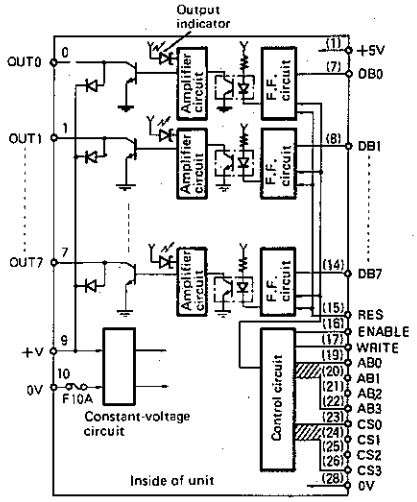
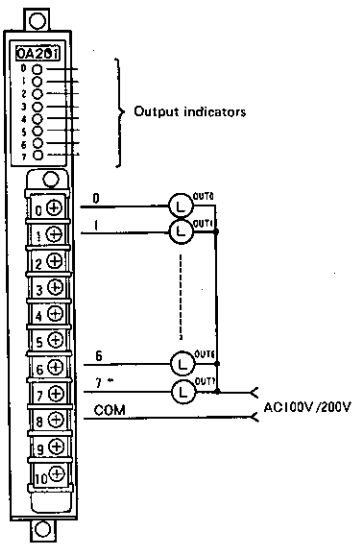
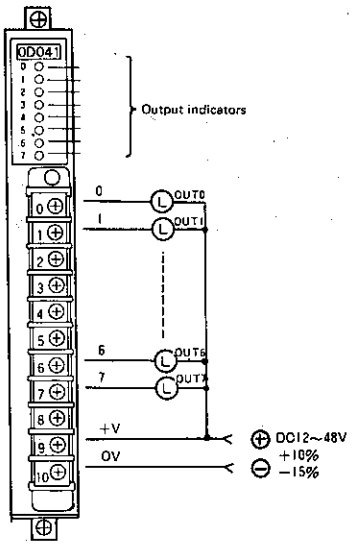
Item \ Type	DC input unit	
	Type SCYM1-ID011	Type SCYM1-ID022
Input voltage	DC 12V max.	DC 24V +10%, –15%
Input impedance	Approx. 1kΩ	Approx. 2kΩ
Input current	2 to 12mA	12mA/point
ON-delay time*	1 to 3msec. (Typ. 2msec.)	5 to 15msec. (Typ. 10msec.)
OFF-delay time**	1 to 5msec. (Typ. 2.5msec.)	15 to 35msec. (Typ. 25msec.)
Number of circuits	8	8
Weight	220g ±5%	220g ±5%
OFF current	0.2mA min.	4.8V min.
Internal circuit		
Terminal connections		

NOTES: * The delay time from the application of an input signal until the activation of the output terminal of the unit.
** The delay time from removal of the input signal until the inactivation of the output terminal of the unit.

- **Output units**

Item \ Type	Contact output unit Type SCY/M1-OC203
Output switching capacity	Contact output AC 250V/DC 24V 2A 10A/unit*
Relay driving voltage	DC 24V +10%, −5% Ripple: within 10%
Relay driving current	23.6mA/point, 215mA max./unit
ON-delay time**	15msec. max.
OFF-delay time***	25msec. max.
Number of circuits	8
Weight	370g ±5%
Current consumption of internal constant-voltage circuit	36mA max. at DC 24V (except the load)
Max. switching frequency	30 operations/minute max. (Minimum switching interval: 2sec. min.)
Service life	Electrically (Under rated load) AC: 200,000 operations DC: 900,000 operations Mechanically 2,000,000 operations
Internal circuit	
Terminal connections	

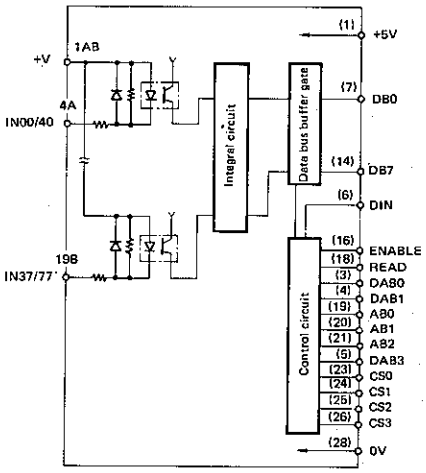
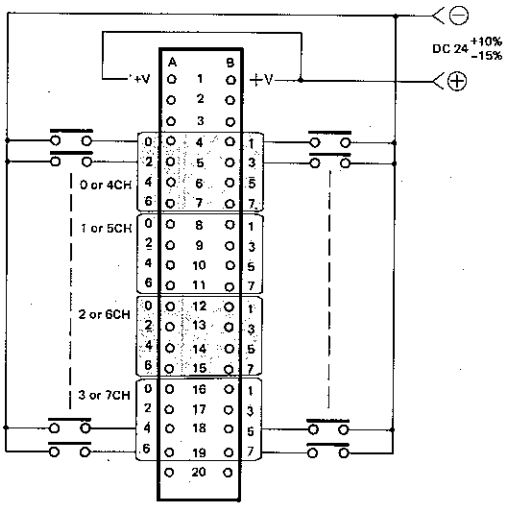
NOTES: * Maximum rating allowable for No. 8 (COM) terminal.
** The delay time from the application of an input signal until the activation of the output terminal of the unit.
*** The delay time from removal of the input signal until the inactivation of the output terminal of the unit.

Item \ Type	Triac output unit Type SCYM1-OA201	Transistor output unit Type SCYM1-OD041
Max. switching capacity	Triac output AC 100 to 200V 1A/point Peak: 8A (10msec max.)/point Max.: 5A/unit*	Transistor output DC 52.8V 500mA
Min. switching capacity	10mA (AC 100V), 20mA (AC 200V)	—
Leakage current	AC 100V 3mA max., AC 200V 6mA max. 60Hz	100μA max.
Saturation voltage	1.2V max. (RMS value) at 1A load	1.5V max.
Supply voltage to internal constant voltage circuit	—	+V: DC 12 to 48V +10%, −15%
Current consumption of internal constant voltage circuit	—	50mA max. at DC 48V (except the load)
ON-delay time	½ load frequency max. (zero crossing circuit incorporated)	0.2msec. max. (resistive load)
OFF-delay time	½ Load frequency max. (zero crossing circuit incorporated)	3msec. max. (resistive load)
Number of circuits	8	8
Weight	325g ±5%	260g ±5%
Fuse capacity	—	—
Internal circuit	 A surge suppressor (varistor) is incorporated in parallel with the triac to protect the triac from external surges.	
Terminal connections		

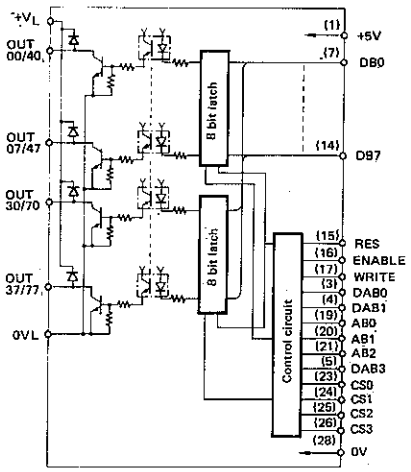
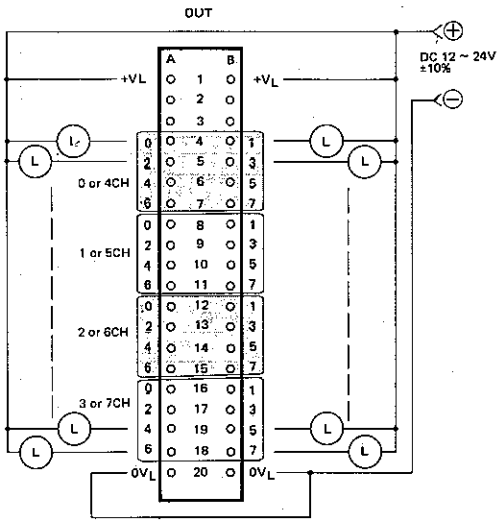
NOTES: * Maximum rating allowable for No. 8 (COM) terminal.
** The delay time from the application of an input signal until the activation of the output terminal of the unit.
*** The delay time from removal of the input signal until the inactivation of the output terminal of the unit.

■ DATA I/O (D I/O) UNITS

● Input units

Item \ Type	DC input unit Type SCYV1-D1021
Input voltage	DC 24V $^{+10\%}_{-15\%}$
Input impedance	≒ 6KΩ
Input current	≒ 4mA
ON-delay time	1.5ms max.
OFF-delay time	2.0ms max.
Number of circuits	32
Weight	300g ±5%
OFF voltage	7V min.
Internal circuit	
Terminal connections	 0 to 3 or 4 to 7CH are governed by the inserting position of the D I/O unit into the expansion I/O base unit. Refer to "3.2 Determination of I/O Relay Numbers."

• Output unit

Item \ Type	DC output unit Type SCY M1-DO021
Max. switching ability	Transistor output DC 24V +10% 100mA/point
Leakage current	1.0μA max.
Saturation voltage	1.2V max. (DC 24V at 100mA)
Supply voltage to internal constant voltage circuit	$+V_L$: DC 12 ~ 24V ±10%
ON-delay time	0.1msec. max. (resistive load)
OFF-delay time	2msec. max. (resistive load)
Number of circuits	32
Weight	300g ±5%
Internal circuit	
Terminal connections	 0 to 3 or 4 to 7CH are governed by the inserting position of the D I/O unit into the expansion I/O base unit. Refer to "3.2 Determination of I/O relay numbers."

■ HIGH-SPEED COUNTER I/O UNITS

- **Features**
- Displays the present count value on the 7-segment LED.
- External and internal signals are isolated by a photocoupler.
- Directly outputs comparison results to the external terminals on the front of the unit. Output signals up to DC 24V 100mA can be driven.
- Both command input and phase differential input can be used as count inputs (selectable by DIP switch settings).
- SYSMAC-M1R can fetch the following status information in addition to the present count value.
  - A coincidence flag
  - A=
  - A>
  - B coincidence flag
  - B=
  - B>

■ **Ratings**

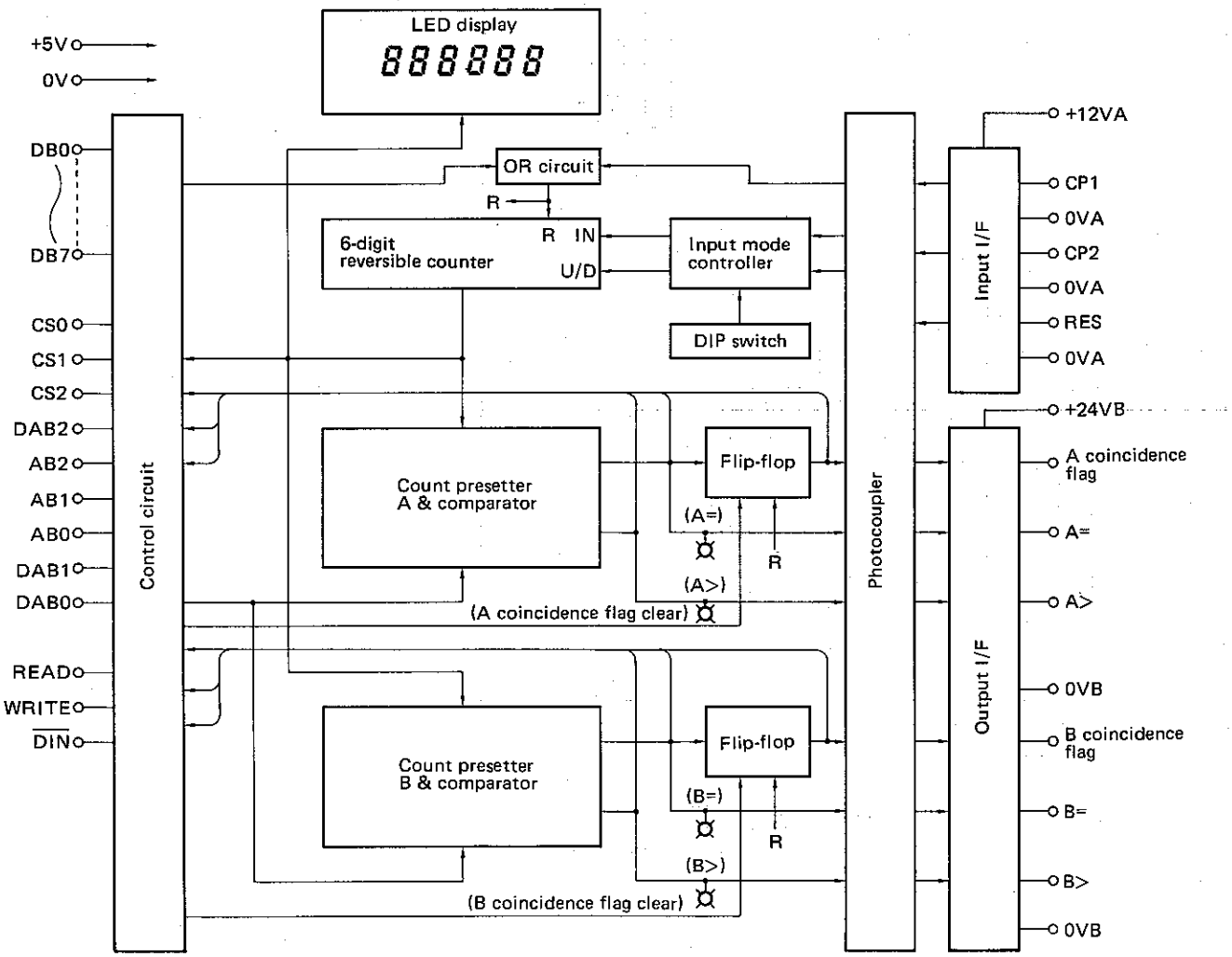
Input signal (Count input, Reset input)	ON level: 6V to 12V OFF level: 0V to 2V
Max. counting speed (Count input)	10kcps
Input response (Reset input)	ON delay: 20msec max. OFF delay: 20msec max.
Input mode	Command input or differential input (selectable by DIP switch settings)
Output signal	DC24V 100mA transistor output (open collector)
Output ON voltage	1.5V max.
Current dissipation	120mA (at 5V)
Weight	670g max.

- **Specifications**

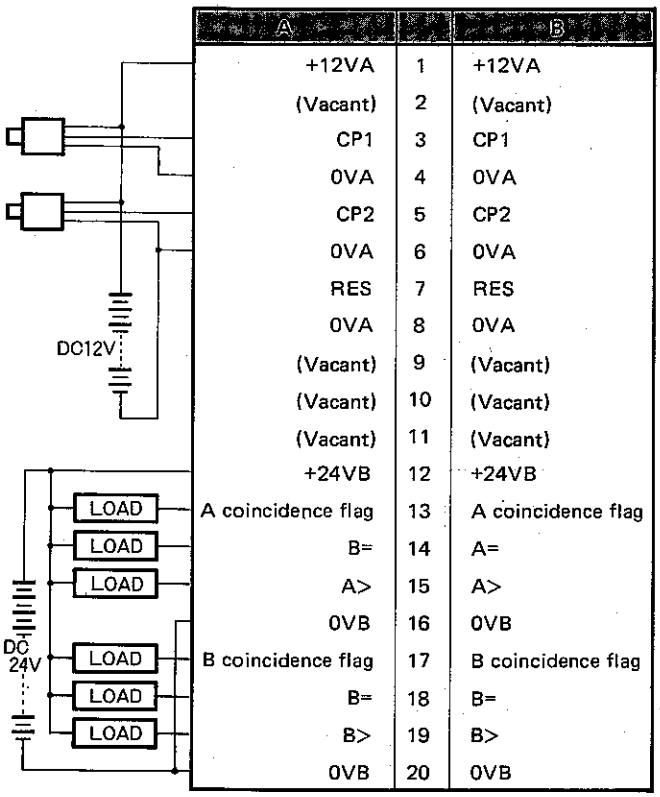
■ **General Specifications**

Conform with SYSMAC-M1R.

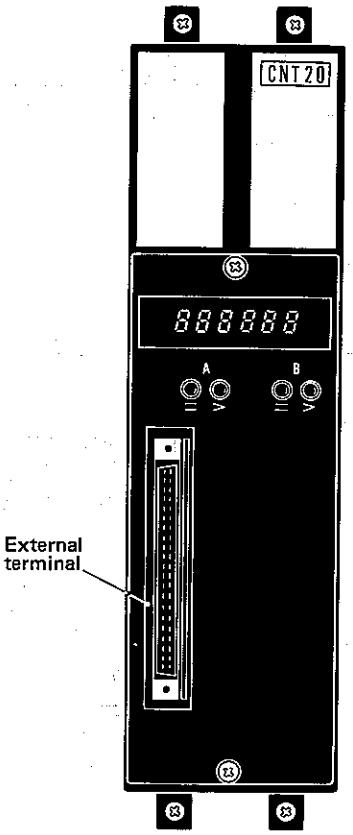
- **Internal circuit**



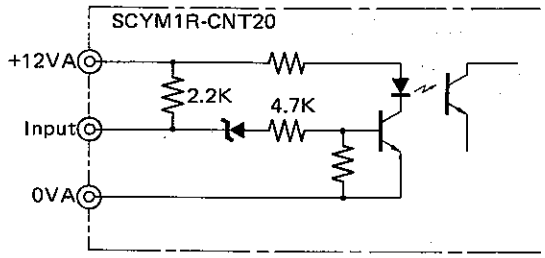
- **External terminal connections**



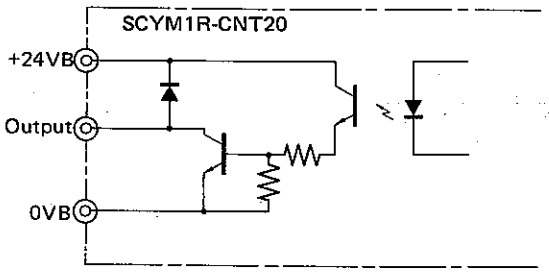
A		B
+12VA	1	+12VA
(Vacant)	2	(Vacant)
CP1	3	CP1
0VA	4	0VA
CP2	5	CP2
0VA	6	0VA
RES	7	RES
0VA	8	0VA
(Vacant)	9	(Vacant)
(Vacant)	10	(Vacant)
(Vacant)	11	(Vacant)
+24VB	12	+24VB
A coincidence flag	13	A coincidence flag
B=	14	A=
A>	15	A>
0VB	16	0VB
B coincidence flag	17	B coincidence flag
B=	18	B=
B>	19	B>
0VB	20	0VB



- **Input Signals**
  Count inputs (CP1 and CP2) and Reset input (RES)



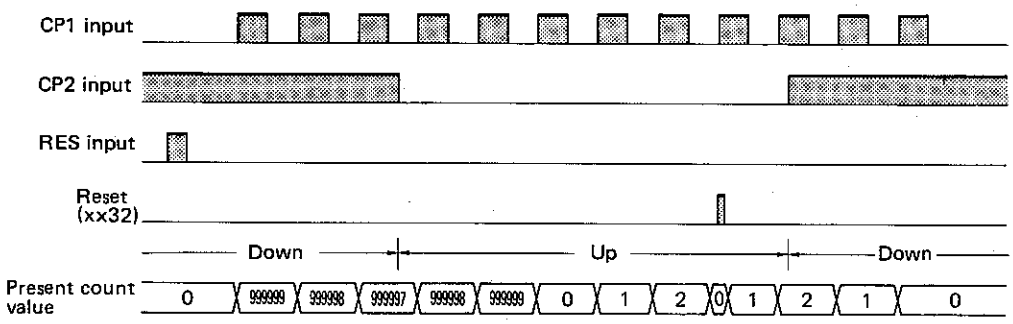
- **Output Signals**
  A coincidence flag, A=, A>, B coincidence flag, B= and B>



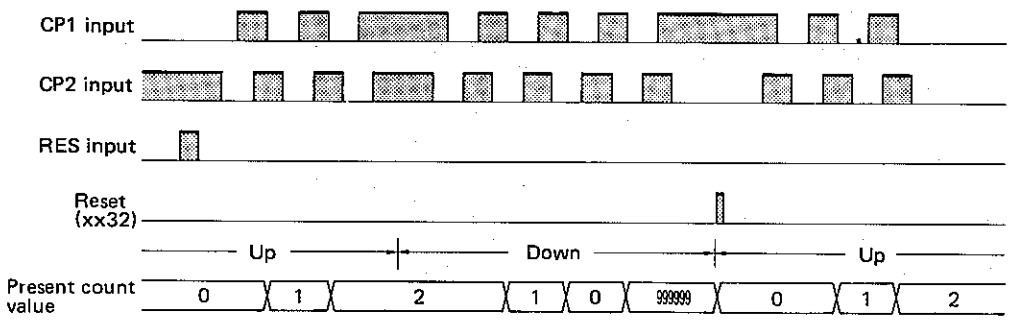
● Operation charts

■ Input Mode

- **Command input mode**



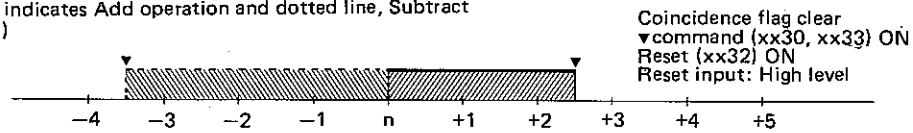
- **Phase differential input mode**



■ Output Mode

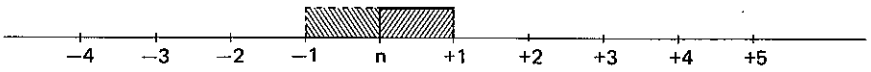
- **A and B coincidence flags**

These flags are output after the present count value coincides with the values of presetters A and B, respectively, until they are reset by A and B coincidence flag clear commands or Reset signal. (Bold line indicates Add operation and dotted line, Subtract operation.)



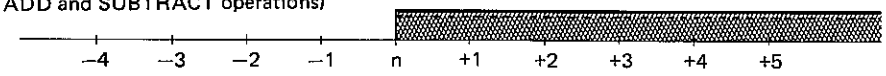
- **A= and B=**

These signals are continuously output while the present count value is equal to the values of presetters A and B, respectively. (Bold line indicates Add operation and dotted line, Subtract operation.)



- **A> and B>**

These signals are continuously output while the present count value is greater than the values of presetter A and B, respectively. (Both in ADD and SUBTRACT operations)



■ A/D CONVERSION INPUT UNIT

- **Features**
- Analog input level display with two 12-split bargraph type LEDs.
- Analog and digital signals are isolated by a photocoupler.
- Converted signals are BCD coded to facilitate arithmetic operations.

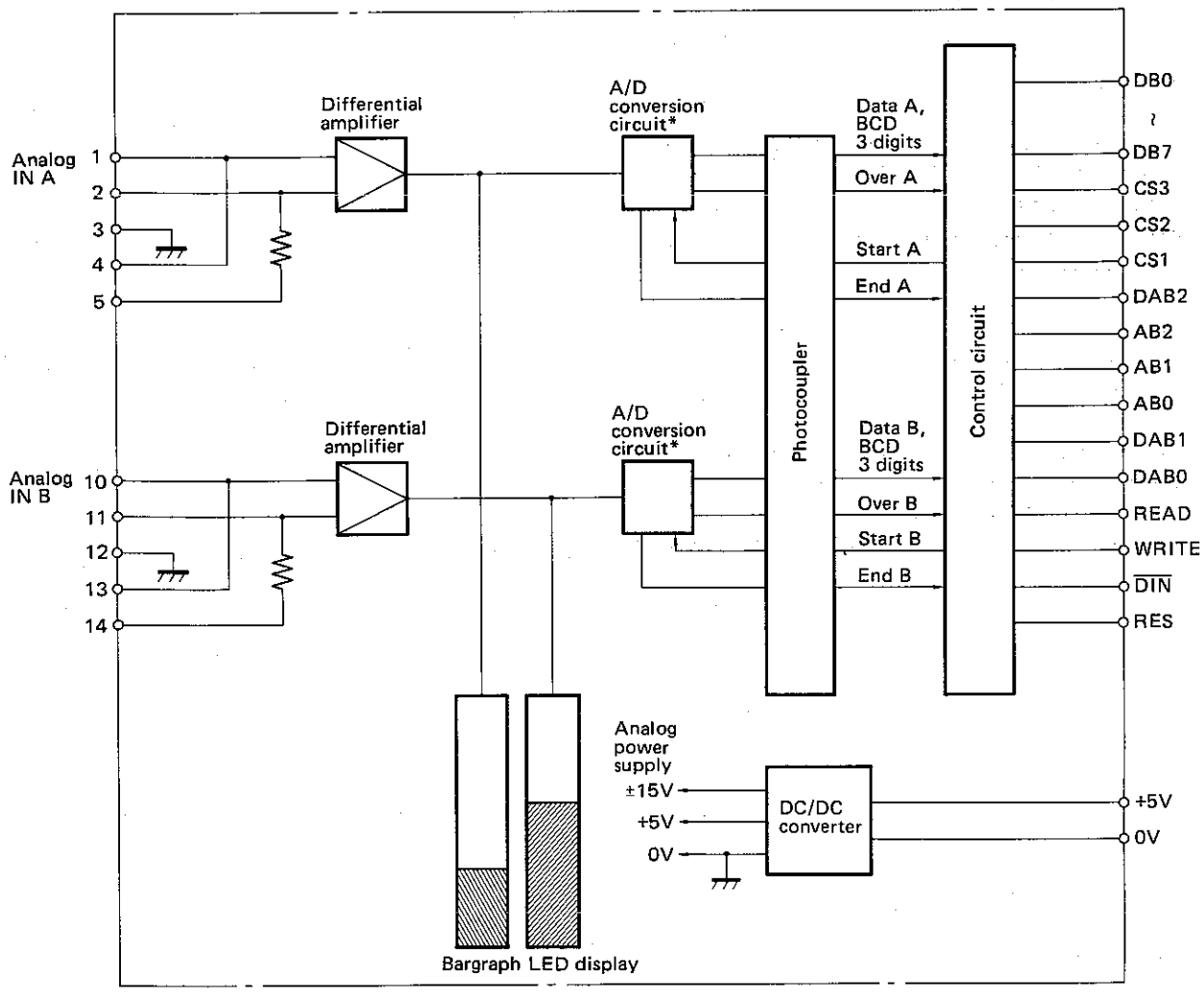
- **Specifications**

▪ **General Specifications**
Conform with SYSMAC-M1R.

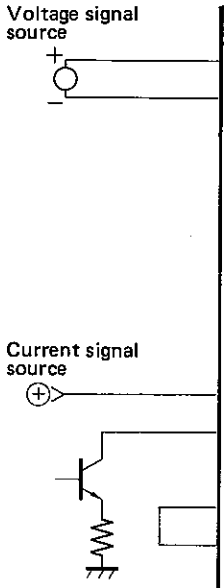
▪ **Ratings**

Input range	Voltage input: +1 to +5V Current input: 4 to 20mA
Output code	3-digit BCD code
Resolution	1/1,000
Accuracy	±3% max. of full scale (at 25° C)
Temp. coefficient	±200PM/°C
Input impedance	Voltage input: 1MΩ min. Current input: 250Ω
Max. permissible input	+15V, −15V
Conversion mode	Integration
Conversion time	15msec max. (in A/D conversion circuit* only)
Input channel	2 channels
Display	2 bargraph LEDs
Current dissipation	0.6A (at 5V)
Weight	770g max.

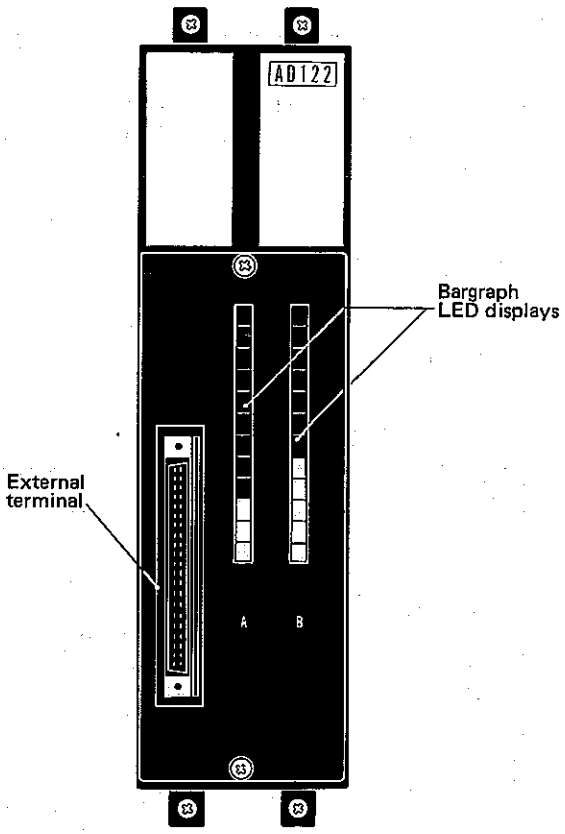
- **Internal circuit**



- **External terminal connections**



A		B
IN A(+)	1	IN A(+)
IN A (–)	2	IN A(–)
GND	3	GND
Current input select	4	Current input select
Current input select	5	Current input select
(Vacant)	6	(Vacant)
(Vacant)	7	(Vacant)
(Vacant)	8	(Vacant)
(Vacant)	9	(Vacant)
IN B(+)	10	IN B(+)
IN B(–)	11	IN B(–)
GND	12	GND
Current input select	13	Current input select
Current input select	14	Current input select
(Vacant)	15	(Vacant)
(Vacant)	16	(Vacant)
(Vacant)	17	(Vacant)
(Vacant)	18	(Vacant)
(Vacant)	19	(Vacant)
(Vacant)	20	(Vacant)

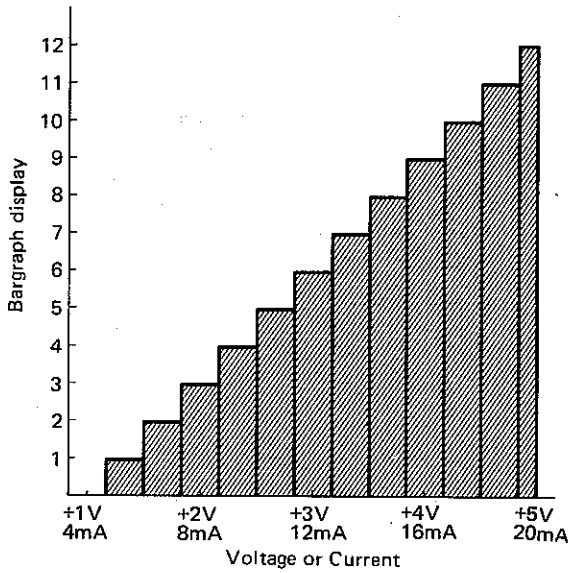


NOTES:
1. 2-conductor twisted, shielded cable should be used for wiring. This cable should be kept separated from other power lines, signal lines, etc. Shielded cable sheath should be grounded.
2. Current input is recommended if a considerable length of wiring is involved.
3. Pay attention to the polarity of input signals.

In case of voltage input, it is unnecessary to short-circuit pins 4 and 5 for IN A and pins 13 and 14 for IN B. In case of current input, short-circuit these pins. In the above connection diagram, IN A is used for voltage input and IN B for current input.

- **Bargraph LED display**

The level of an analog signal input is displayed for each channel using a 12-split bargraph type LED. The bargraph display represents the approximate input level which serves for your reference only. The illuminating state of the LED display is shown on the right.
All bargraphs are extinguished at the minimum level of +1V or 4mA and are illuminated at the maximum level of +5V or 20mA.



■ D/A CONVERSION OUTPUT UNIT

- **Features**
- Analog output level display with two 12-split bargraph type LEDs.
- Analog and digital signals are isolated by a photocoupler. The power supply is isolated by an isolated type DC-DC converter.
- Digital signals for conversion are BCD codes to facilitate arithmetic operations.

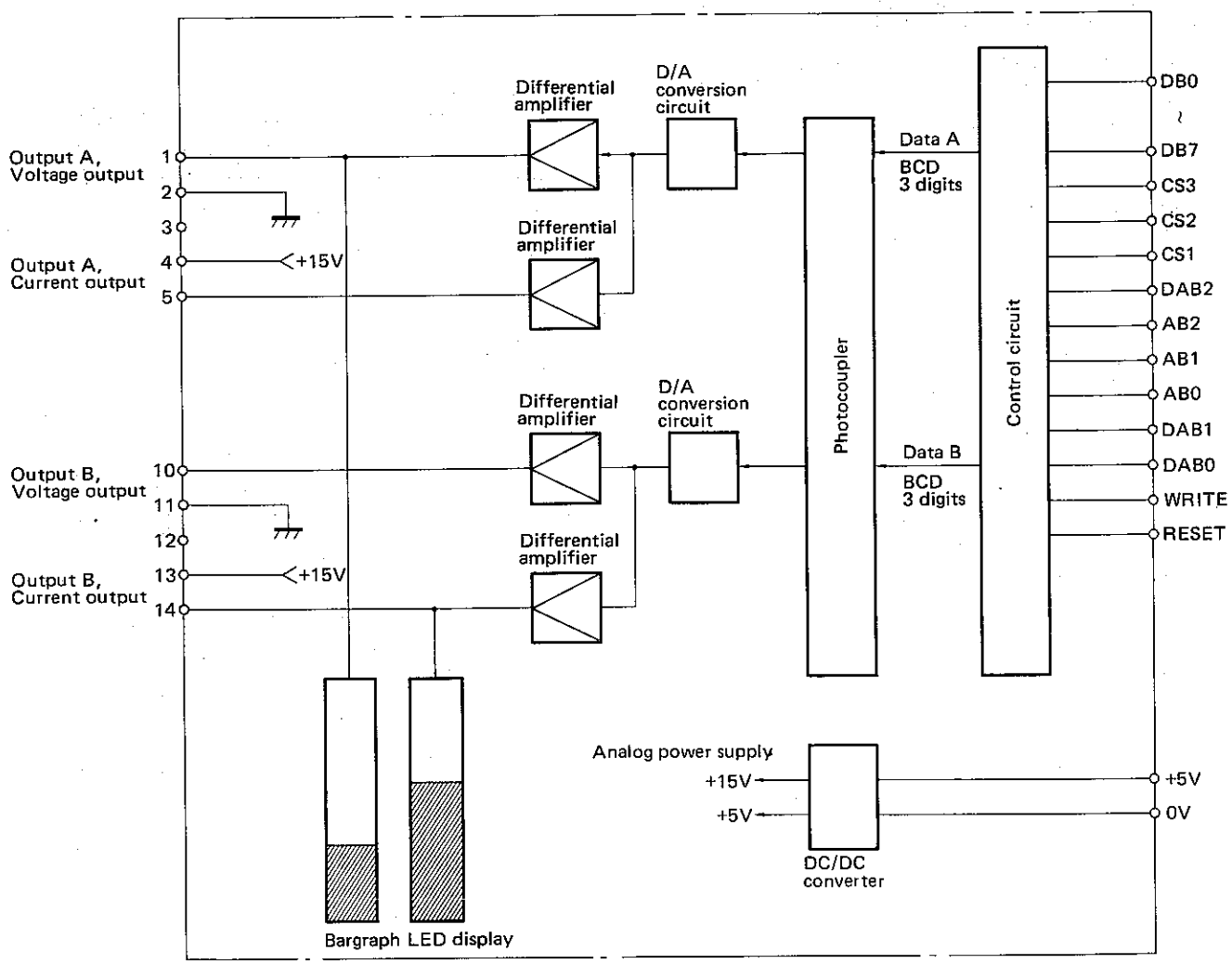
- **Specifications**

▪ **General Specifications**
Conform with SYSMAC-M1R.

▪ **Ratings**

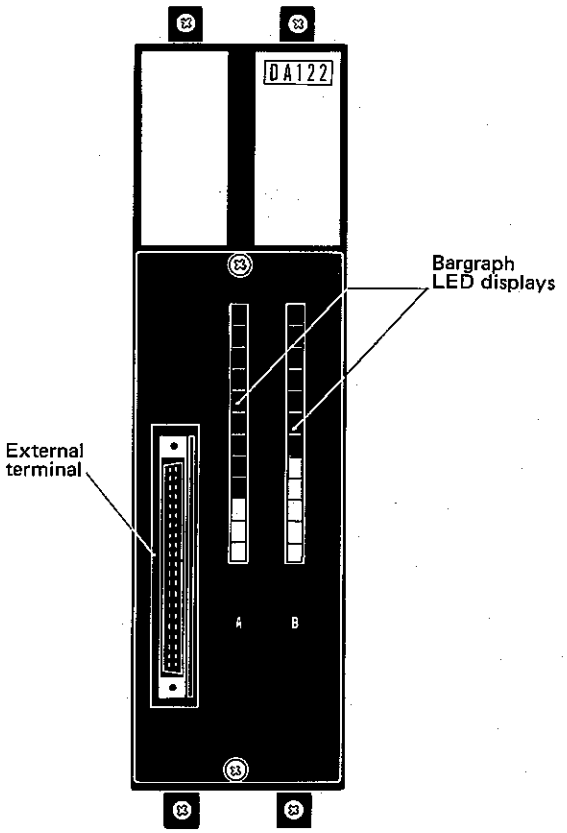
Output range	Voltage output: +1 to +5V Current output: 4 to 20mA
Input code	BCD 3-digit code
Resolution	1/1,000
Accuracy	±3% max. of full scale (at 25° C)
Temp. coefficient	±100PPM/°C
Output impedance	0.5Ω max.
Max. output current	15mA (in voltage output)
Conversion time	2msec max.
Output channel	2 channels
Display	2 bargraph LEDs
Current dissipation	1.4A (at 5V)
Weight	680g max.

- **Internal circuit**



• External terminal connections

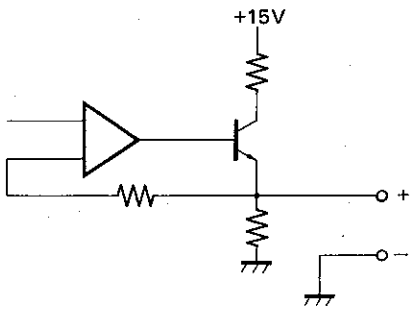
A		B
Voltage output A (+)	1	Voltage output A (+)
Voltage output A (—)	2	Voltage output A (—)
(Vacant)	3	(Vacant)
Current output (+)	4	Current output (+)
Current output (—)	5	Current output (—)
(Vacant)	6	(Vacant)
(Vacant)	7	(Vacant)
(Vacant)	8	(Vacant)
(Vacant)	9	(Vacant)
Voltage output B (+)	10	Voltage output B (+)
Voltage output B (—)	11	Voltage output B (—)
(Vacant)	12	(Vacant)
Current output (+)	13	Current output (+)
Current output (—)	14	Current output (—)
(Vacant)	15	(Vacant)
(Vacant)	16	(Vacant)
(Vacant)	17	(Vacant)
(Vacant)	18	(Vacant)
(Vacant)	19	(Vacant)
(Vacant)	20	(Vacant)



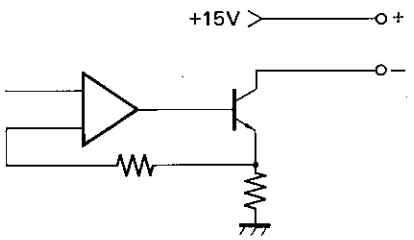
NOTES:
1. 2-conductor twisted, shielded cable must be used for wiring. This cable should be kept separated from other power lines and signal lines.
2. Pay attention to the polarity of output signals.
3. Current output is recommended if a considerable length of wiring is involved.

• Output mode

▪ Voltage Output

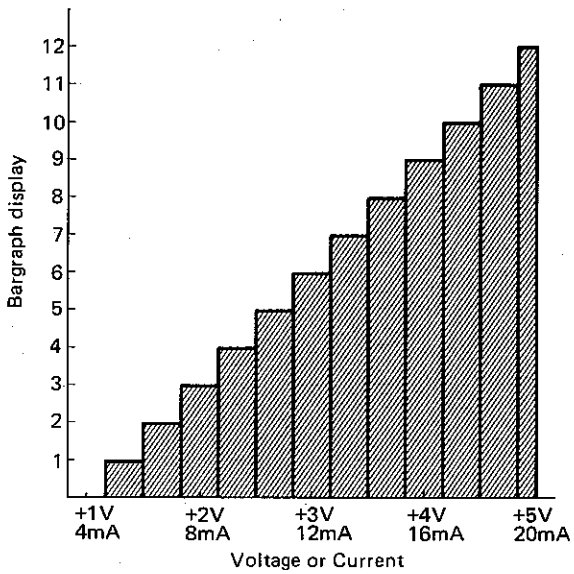


▪ Current Output



• Bargraph LED display

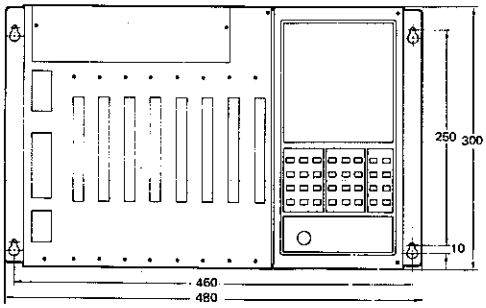
The level of an analog signal output is displayed for each channel using a 12-split bargraph type LED. The bargraph display represents the approximate output level for your reference only. The illuminating state of the LED display is as shown below.



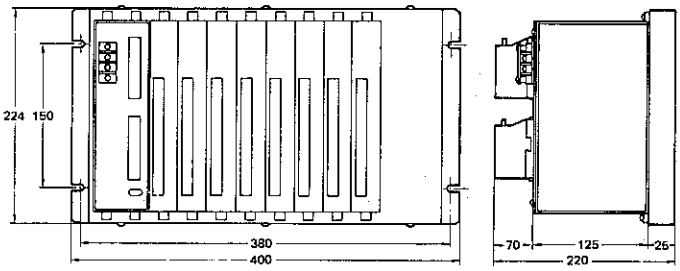
All bargraphs are extinguished at the minimum level of +1V or 4mA and are illuminated at the maximum level of +5V or 20mA.

2.4 Dimensions

- **CPU rack**

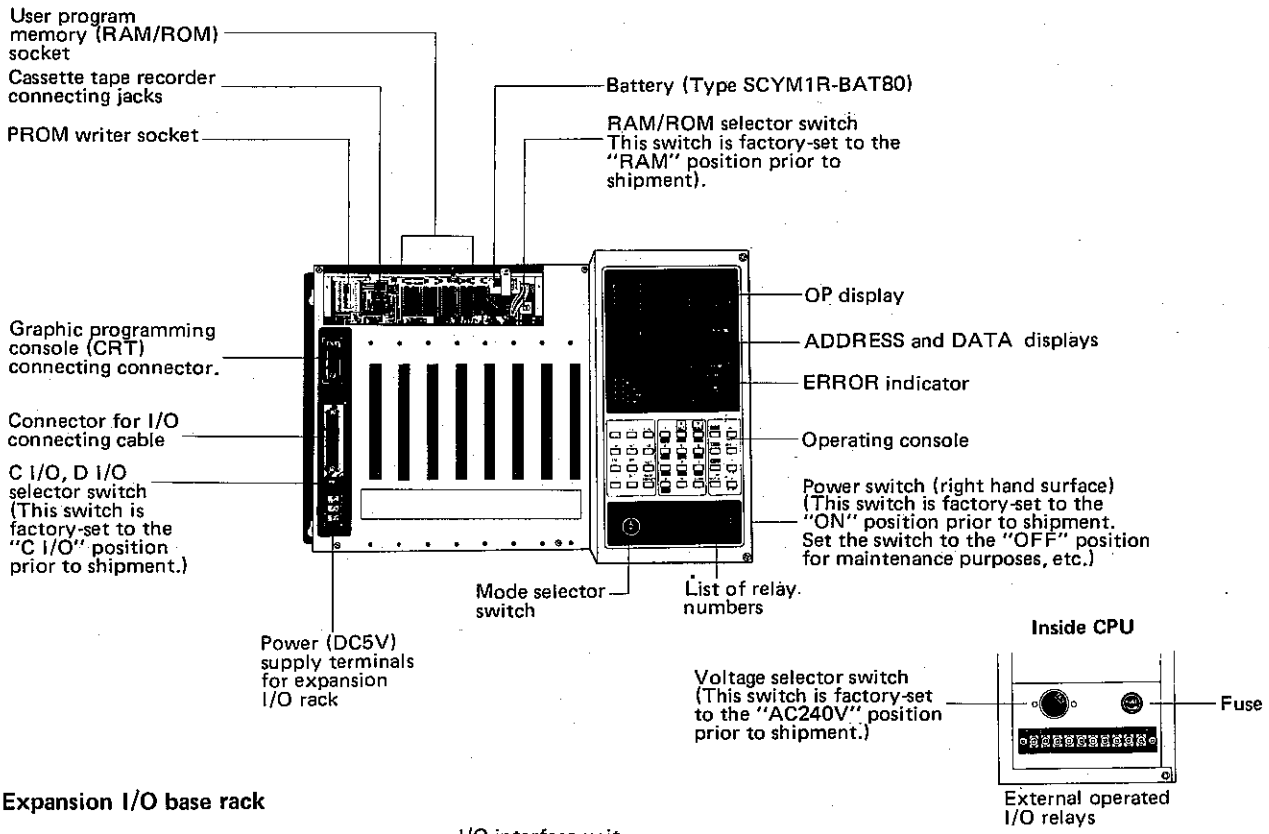


- **Expansion I/O rack**

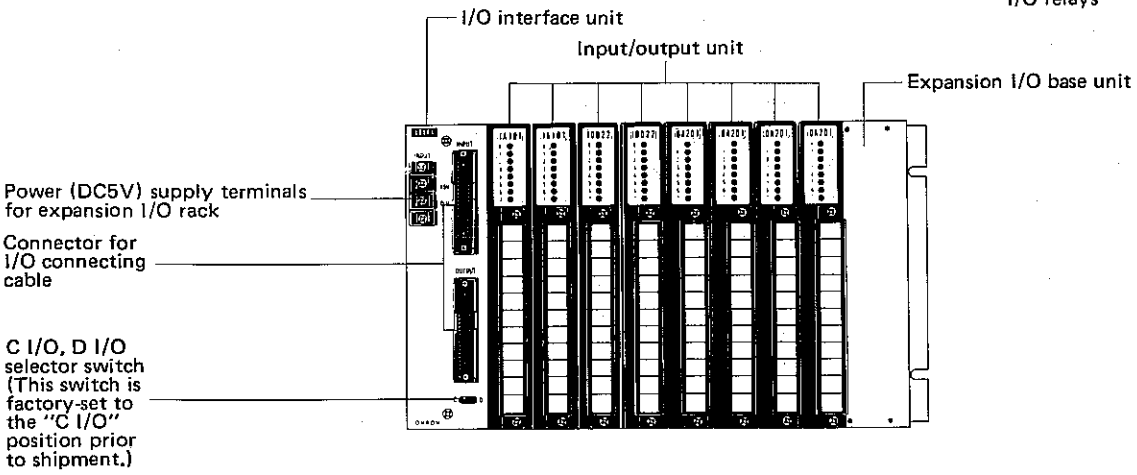


2.5 Names of Respective Parts

- **CPU rack**



- **Expansion I/O base rack**



3. Assignment of Relay Numbers

Relay numbers correspond to the data memory areas and the operating state (ON/OFF) of each relay is stored in the corresponding memory area.
The method of assigning relay numbers used for the SYSMAC-M1R is as follows.

3.1 List of Relay Numbers

Name	No. of points	Symbol	Relay number														
Input/output relay	512	—	0000	0010	0020	0030	0040	0050	0060	0070	0100	0110	0120	0130	0140	0150	0160	0170
			0001	0011	0021	0031	0041	0051	0061	0071	0101	0111	0121	0131	0141	0151	0161	0171
			0002	0012	0022	0032	0042	0052	0062	0072	0102	0112	0122	0132	0142	0152	0162	0172
			0003	0013	0023	0033	0043	0053	0063	0073	0103	0113	0123	0133	0143	0153	0163	0173
			0004	0014	0024	0034	0044	0054	0064	0074	0104	0114	0124	0134	0144	0154	0164	0174
			0005	0015	0025	0035	0045	0055	0065	0075	0105	0115	0125	0135	0145	0155	0165	0175
			0006	0016	0026	0036	0046	0056	0066	0076	0106	0116	0126	0136	0146	0156	0166	0176
			0007	0017	0027	0037	0047	0057	0067	0077	0107	0117	0127	0137	0147	0157	0167	0177
			0200	0210	0220	0230	0240	0250	0260	0270	0300	0310	0320	0330	0340	0350	0360	0370
			0201	0211	0221	0231	0241	0251	0261	0271	0301	0311	0321	0331	0341	0351	0361	0371
			0202	0212	0222	0232	0242	0252	0262	0272	0302	0312	0322	0332	0342	0352	0362	0372
			0203	0213	0223	0233	0243	0253	0263	0273	0303	0313	0323	0333	0343	0353	0363	0373
			0204	0214	0224	0234	0244	0254	0264	0274	0304	0314	0324	0334	0344	0354	0364	0374
			0205	0215	0225	0235	0245	0255	0265	0275	0305	0315	0325	0335	0345	0355	0365	0375
			0206	0216	0226	0236	0246	0256	0266	0276	0306	0316	0326	0336	0346	0356	0366	0376
			0207	0217	0227	0237	0247	0257	0267	0277	0307	0317	0327	0337	0347	0357	0367	0377
			0400	0410	0420	0430	0440	0450	0460	0470	0500	0510	0520	0530	0540	0550	0560	0570
			0401	0411	0421	0431	0441	0451	0461	0471	0501	0511	0521	0531	0541	0551	0561	0571
			0402	0412	0422	0432	0442	0452	0462	0472	0502	0512	0522	0532	0542	0552	0562	0572
			0403	0413	0423	0433	0443	0453	0463	0473	0503	0513	0523	0533	0543	0553	0563	0573
			0404	0414	0424	0434	0444	0454	0464	0474	0504	0514	0524	0534	0544	0554	0564	0574
			0405	0415	0425	0435	0445	0455	0465	0475	0505	0515	0525	0535	0545	0555	0565	0575
			0406	0416	0426	0436	0446	0456	0466	0476	0506	0516	0526	0536	0546	0556	0566	0576
			0407	0417	0427	0437	0447	0457	0467	0477	0507	0517	0527	0537	0547	0557	0567	0577
			0600	0610	0620	0630	0640	0650	0660	0670	0700	0710	0720	0730	0740	0750	0760	0770
			0601	0611	0621	0631	0641	0651	0661	0671	0701	0711	0721	0731	0741	0751	0761	0771
			0602	0612	0622	0632	0642	0652	0662	0672	0702	0712	0722	0732	0742	0752	0762	0772
			0603	0613	0623	0633	0643	0653	0663	0673	0703	0713	0723	0733	0743	0753	0763	0773
			0604	0614	0624	0634	0644	0654	0664	0674	0704	0714	0724	0734	0744	0754	0764	0774
			0605	0615	0625	0635	0645	0655	0665	0675	0705	0715	0725	0735	0745	0755	0765	0775
			0606	0616	0626	0636	0646	0656	0666	0676	0706	0716	0726	0736	0746	0756	0766	0776
			0607	0617	0627	0637	0647	0657	0667	0677	0707	0717	0727	0737	0747	0757	0767	0777
Internal auxiliary relay	224	—	1000	1010	1020	1030	1040	1050	1060	1070	1100	1110	1120	1130	1140	1150	1160	1170
			1001	1011	1021	1031	1041	1051	1061	1071	1101	1111	1121	1131	1141	1151	1161	1171
			1002	1012	1022	1032	1042	1052	1062	1072	1102	1112	1122	1132	1142	1152	1162	1172
			1003	1013	1023	1033	1043	1053	1063	1073	1103	1113	1123	1133	1143	1153	1163	1173
			1004	1014	1024	1034	1044	1054	1064	1074	1104	1114	1124	1134	1144	1154	1164	1174
			1005	1015	1025	1035	1045	1055	1065	1075	1105	1115	1125	1135	1145	1155	1165	1175
			1006	1016	1026	1036	1046	1056	1066	1076	1106	1116	1126	1136	1146	1156	1166	1176
			1007	1017	1027	1037	1047	1057	1067	1077	1107	1117	1127	1137	1147	1157	1167	1177
			1200	1210	1220	1230	1240	1250	1260	1270	1300	1310	1320	1330	1340	1350	1360	1370
			1201	1211	1221	1231	1241	1251	1261	1271	1301	1311	1321	1331	1341	1351	1361	1371
			1202	1212	1222	1232	1242	1252	1262	1272	1302	1312	1322	1332	1342	1352	1362	1372
			1203	1213	1223	1233	1243	1253	1263	1273	1303	1313	1323	1333	1343	1353	1363	1373
			1204	1214	1224	1234	1244	1254	1264	1274	1304	1314	1324	1334	1344	1354	1364	1374
			1205	1215	1225	1235	1245	1255	1265	1275	1305	1315	1325	1335	1345	1355	1365	1375
			1206	1216	1226	1236	1246	1256	1266	1276	1306	1316	1326	1336	1346	1356	1366	1376
			1207	1217	1227	1237	1247	1257	1267	1277	1307	1317	1327	1337	1347	1357	1367	1377

Special auxiliary relay area

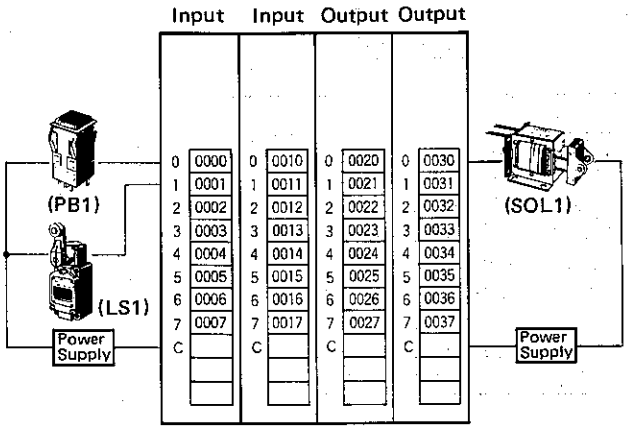
Name	No. of points	Symbol	Relay number															
Timer and counter	128	TIM CNT	000	010	020	030	040	050	060	070	100	110	120	130	140	150	160	170
			001	011	021	031	041	051	061	071	101	111	121	131	141	151	161	171
			002	012	022	032	042	052	062	072	102	112	122	132	142	152	162	172
			003	013	023	033	043	053	063	073	103	113	123	133	143	153	163	173
			004	014	024	034	044	054	064	074	104	114	124	134	144	154	164	174
			005	015	025	035	045	055	065	075	105	115	125	135	145	155	165	175
			006	016	026	036	046	056	066	076	106	116	126	136	146	156	166	176
			007	017	027	037	047	057	067	077	107	117	127	137	147	157	167	177
Latching relay	256	KR	000	010	020	030	040	050	060	070	100	110	120	130	140	150	160	170
			001	011	021	031	041	051	061	071	101	111	121	131	141	151	161	171
			002	012	022	032	042	052	062	072	102	112	122	132	142	152	162	172
			003	013	023	033	043	053	063	073	103	113	123	133	143	153	163	173
			004	014	024	034	044	054	064	074	104	114	124	134	144	154	164	174
			005	015	025	035	045	055	065	075	105	115	125	135	145	155	165	175
			006	016	026	036	046	056	066	076	106	116	126	136	146	156	166	176
			007	017	027	037	047	057	067	077	107	117	127	137	147	157	167	177
			200	210	220	230	240	250	260	270	300	310	320	330	340	350	360	370
			201	211	221	231	241	251	261	271	301	311	321	331	341	351	361	371
			202	212	222	232	242	252	262	272	302	312	322	332	342	352	362	372
			203	213	223	233	243	253	263	273	303	313	323	333	343	353	363	373
			204	214	224	234	244	254	264	274	304	314	324	334	344	354	364	374
			205	215	225	235	245	255	265	275	305	315	325	335	345	355	365	375
			206	216	226	236	246	256	266	276	306	316	326	336	346	356	366	376
			207	217	227	237	247	257	267	277	307	317	327	337	347	357	367	377
Shift register	8 bits x 32	SR	000	010	020	030	040	050	060	070	100	110	120	130	140	150	160	170
			001	011	021	031	041	051	061	071	101	111	121	131	141	151	161	171
			002	012	022	032	042	052	062	072	102	112	122	132	142	152	162	172
			003	013	023	033	043	053	063	073	103	113	123	133	143	153	163	173
			004	014	024	034	044	054	064	074	104	114	124	134	144	154	164	174
			005	015	025	035	045	055	065	075	105	115	125	135	145	155	165	175
			006	016	026	036	046	056	066	076	106	116	126	136	146	156	166	176
			007	017	027	037	047	057	067	077	107	117	127	137	147	157	167	177
			200	210	220	230	240	250	260	270	300	310	320	330	340	350	360	370
			201	211	221	231	241	251	261	271	301	311	321	331	341	351	361	371
			202	212	222	232	242	252	262	272	302	312	322	332	342	352	362	372
			203	213	223	233	243	253	263	273	303	313	323	333	343	353	363	373
			204	214	224	234	244	254	264	274	304	314	324	334	344	354	364	374
			205	215	225	235	245	255	265	275	305	315	325	335	345	355	365	375
			206	216	226	236	246	256	266	276	306	316	326	336	346	356	366	376
			207	217	227	237	247	257	267	277	307	317	327	337	347	357	367	377
Temporary memory relay	8	TR	0	1	2	3	4	5	6	7								

Name	No. of points	Symbol	Relay number		Description
Special auxiliary relay	28	—	1340 1341 1342 1343	2^0 2^1 2^2 2^3	$X10^0$ (Low-order digit)
			1344 1345 1346 1347	2^0 2^1 2^2 2^3	$X10^1$ (High-order digit)
					The FAL NO. (00~99) when the Diagnostic (FAL) instruction is executed, is output in BCD to each of relay Nos. 1340 to 1347.
			1350 1351 1352 1353	2^0 2^1 2^2 2^3	$X10^0$ (Low-order digit)
			1354 1355 1356 1357	2^0 2^1 2^2 2^3	$X10^1$ (High-order digit)
					The calculation result when the Add (+) or Subtract (−) instruction is executed, is output in BCD to each of relay Nos. 1350 to 1357.
			1360		This relay turns ON if there is a carry in the result when the Addition (+) instruction is executed. This relay also turns ON if there is a borrow in the result when the Subtraction (−) instruction is executed.
			1361		This relay turns ON if the result when the compare (CMP) instruction is executed, is less than (<).
			1362		This relay turns ON if the result when the compare (CMP) instruction is executed, is equal (=).
			1363		This relay turns ON if the result when the compare (CMP) instruction is executed, is more than (>).
			1364		This relay is normally OFF.
			1365		This relay is normally ON.
			1366		This relay is normally OFF.
			1367		This relay is normally ON.
			1370 1371 1372 1373		These 4 relays are not used. Note that the "1" or "0" state of these relays is not clear. However, when the MOV instruction is executed, the 8-bit contents of the relay Nos. 1370 to 1377 will be transferred.
			1374		This relay turns ON when the battery is abnormal.
			1375		This relay is used to generate 0.2sec clock pulse.
			1376		This relay is used to generate 1sec clock pulse.
			1377		This relay is used to generate 0.1sec clock pulse.

3.2 Determination of I/O Relay Numbers

1. In a sequence circuit diagram which is generally known, a sequence circuit is drawn with input/output devices included in the sequence circuit. With the SYSMAC, however, the sequence circuit is configured in such a form that input/output devices will be once accepted by I/O units. For this reason, it is necessary to determine the locations where I/O units are to be inserted into the CPU rack or the expansion I/O rack for each I/O device and the I/O terminals to which I/O devices are to be connected.
2. The ladder diagrams of the SYSMAC-M1R require the relay numbers corresponding to the I/O devices. The relay numbers are determined by the mounting locations of the respective I/O units in the CPU rack or expansion I/O rack to which I/O devices are to be connected and the connecting terminals of the I/O units. Each of these relay numbers must be used for ladder diagrams and programming.

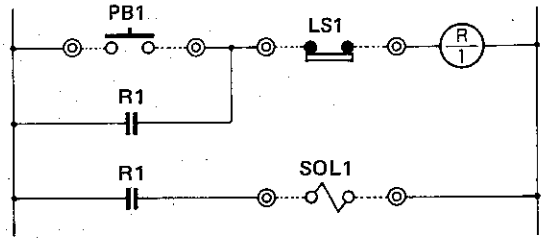
Example of wiring input/output devices



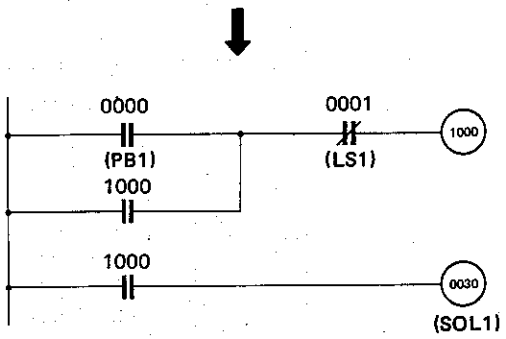
3. When the CPU rack and expansion I/O racks are connected, I/O relay numbers are assigned as follows.

NOTES:
1. The mounting locations of I/O units in the CPU rack or the I/O rack are free. However, the CPU judges whether the unit located in an input unit or an output unit.
2. The relay number of the unit location to which no I/O unit is inserted can be used as an internal auxiliary relay number.
3. The relay number of the unit location to which an input unit is inserted cannot be used as an internal auxiliary relay number.
4. The relay number of the unit location to which an output unit is inserted but no output device is connected, can be used as an internal auxiliary relay. (However, the output relay will turn ON/OFF.)

Circuit example



General sequence circuit

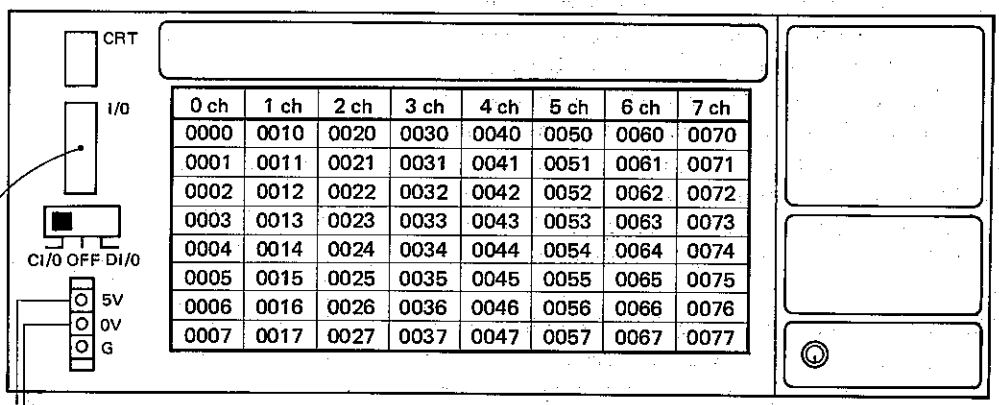


Ladder diagram of
SYSMAC M1R-CPU80 series

- PB1 and LS1 are connected to the input unit while SOL1 is connected to the output unit. R1 employs an internal auxiliary relay (1000). In this case SOL1 may be connected directly to the output unit without using the internal auxiliary relay.

- When C I/O units alone are used.

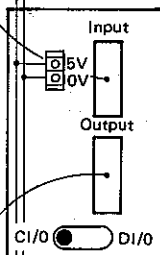
CPU rack



0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0000	0010	0020	0030	0040	0050	0060	0070
0001	0011	0021	0031	0041	0051	0061	0071
0002	0012	0022	0032	0042	0052	0062	0072
0003	0013	0023	0033	0043	0053	0063	0073
0004	0014	0024	0034	0044	0054	0064	0074
0005	0015	0025	0035	0045	0055	0065	0075
0006	0016	0026	0036	0046	0056	0066	0076
0007	0017	0027	0037	0047	0057	0067	0077

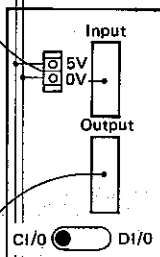
Expansion I/O rack

NO. 1



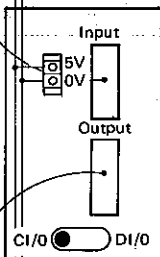
0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0100	0110	0120	0130	0140	0150	0160	0170
0101	0111	0121	0131	0141	0151	0161	0171
0102	0112	0122	0132	0142	0152	0162	0172
0103	0113	0123	0133	0143	0153	0163	0173
0104	0114	0124	0134	0144	0154	0164	0174
0105	0115	0125	0135	0145	0155	0165	0175
0106	0116	0126	0136	0146	0156	0166	0176
0107	0117	0127	0137	0147	0157	0167	0177

NO. 2



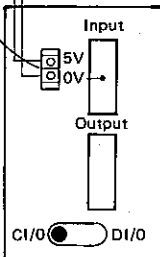
0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0200	0210	0220	0230	0240	0250	0260	0270
0201	0211	0221	0231	0241	0251	0261	0271
0202	0212	0222	0232	0242	0252	0262	0272
0203	0213	0223	0233	0243	0253	0263	0273
0204	0214	0224	0234	0244	0254	0264	0274
0205	0215	0225	0235	0245	0255	0265	0275
0206	0216	0226	0236	0246	0256	0266	0276
0207	0217	0227	0237	0247	0257	0267	0277

NO. 3



0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0300	0310	0320	0330	0340	0350	0360	0370
0301	0311	0321	0331	0341	0351	0361	0371
0302	0312	0322	0332	0342	0352	0362	0372
0303	0313	0323	0333	0343	0353	0363	0373
0304	0314	0324	0334	0344	0354	0364	0374
0305	0315	0325	0335	0345	0355	0365	0375
0306	0316	0326	0336	0346	0356	0366	0376
0307	0317	0327	0337	0347	0357	0367	0377

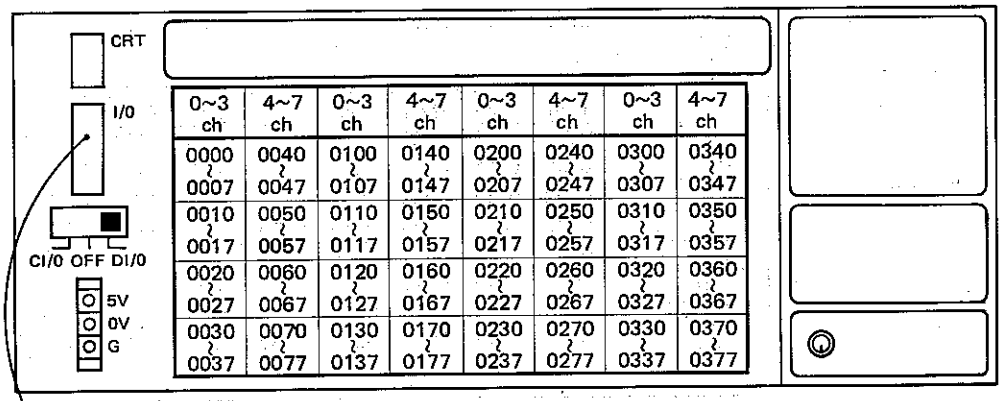
NO. 4



0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0400	0410	0420	0430	0440	0450	0460	0470
0401	0411	0421	0431	0441	0451	0461	0471
0402	0412	0422	0432	0442	0452	0462	0472
0403	0413	0423	0433	0443	0453	0463	0473
0404	0414	0424	0434	0444	0454	0464	0474
0405	0415	0425	0435	0445	0455	0465	0475
0406	0416	0426	0436	0446	0456	0466	0476
0407	0417	0427	0437	0447	0457	0467	0477

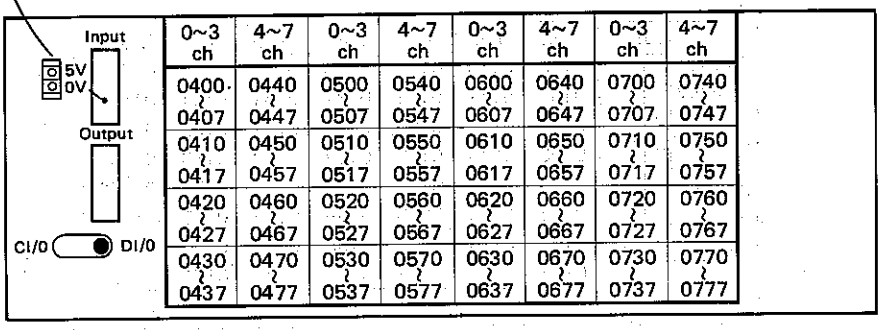
- **When D I/O units alone are used**

CPU rack



0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0000 ~ 0007	0040 ~ 0047	0100 ~ 0107	0140 ~ 0147	0200 ~ 0207	0240 ~ 0247	0300 ~ 0307	0340 ~ 0347
0010 ~ 0017	0050 ~ 0057	0110 ~ 0117	0150 ~ 0157	0210 ~ 0217	0250 ~ 0257	0310 ~ 0317	0350 ~ 0357
0020 ~ 0027	0060 ~ 0067	0120 ~ 0127	0160 ~ 0167	0220 ~ 0227	0260 ~ 0267	0320 ~ 0327	0360 ~ 0367
0030 ~ 0037	0070 ~ 0077	0130 ~ 0137	0170 ~ 0177	0230 ~ 0237	0270 ~ 0277	0330 ~ 0337	0370 ~ 0377

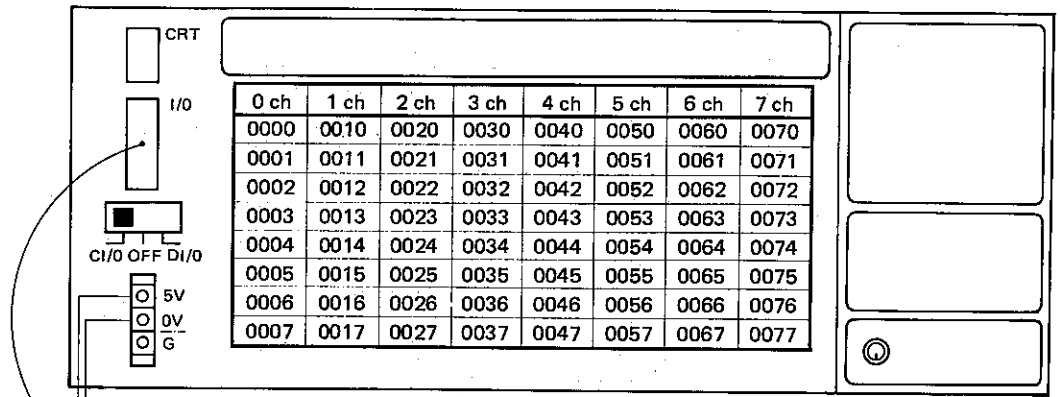
Expansion I/O rack



0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0400 ~ 0407	0440 ~ 0447	0500 ~ 0507	0540 ~ 0547	0600 ~ 0607	0640 ~ 0647	0700 ~ 0707	0740 ~ 0747
0410 ~ 0417	0450 ~ 0457	0510 ~ 0517	0550 ~ 0557	0610 ~ 0617	0650 ~ 0657	0710 ~ 0717	0750 ~ 0757
0420 ~ 0427	0460 ~ 0467	0520 ~ 0527	0560 ~ 0567	0620 ~ 0627	0660 ~ 0667	0720 ~ 0727	0760 ~ 0767
0430 ~ 0437	0470 ~ 0477	0530 ~ 0537	0570 ~ 0577	0630 ~ 0637	0670 ~ 0677	0730 ~ 0737	0770 ~ 0777

- **When C I/O units and D I/O units are used.**

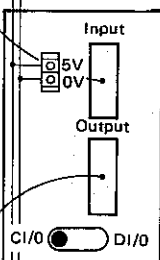
CPU rack
(with C I/O selected)



0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0000	0010	0020	0030	0040	0050	0060	0070
0001	0011	0021	0031	0041	0051	0061	0071
0002	0012	0022	0032	0042	0052	0062	0072
0003	0013	0023	0033	0043	0053	0063	0073
0004	0014	0024	0034	0044	0054	0064	0074
0005	0015	0025	0035	0045	0055	0065	0075
0006	0016	0026	0036	0046	0056	0066	0076
0007	0017	0027	0037	0047	0057	0067	0077

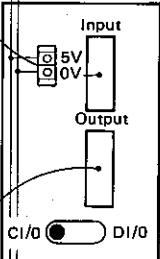
Expansion I/O racks

No. 1
(with C I/O selected)



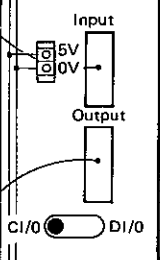
0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0100	0110	0120	0130	0140	0150	0160	0170
0101	0111	0121	0131	0141	0151	0161	0171
0102	0112	0122	0132	0142	0152	0162	0172
0103	0113	0123	0133	0143	0153	0163	0173
0104	0114	0124	0134	0144	0154	0164	0174
0105	0115	0125	0135	0145	0155	0165	0175
0106	0116	0126	0136	0146	0156	0166	0176
0107	0117	0127	0137	0147	0157	0167	0177

No. 2
(with C I/O selected)



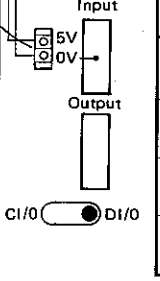
0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0200	0210	0220	0230	0240	0250	0260	0270
0201	0211	0221	0231	0241	0251	0261	0271
0202	0212	0222	0232	0242	0252	0262	0272
0203	0213	0223	0233	0243	0253	0263	0273
0204	0214	0224	0234	0244	0254	0264	0274
0205	0215	0225	0235	0245	0255	0265	0275
0206	0216	0226	0236	0246	0256	0266	0276
0207	0217	0227	0237	0247	0257	0267	0277

No. 3
(with C I/O selected)



0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0300	0310	0320	0330	0340	0350	0360	0370
0301	0311	0321	0331	0341	0351	0361	0371
0302	0312	0322	0332	0342	0352	0362	0372
0303	0313	0323	0333	0343	0353	0363	0373
0304	0314	0324	0334	0344	0354	0364	0374
0305	0315	0325	0335	0345	0355	0365	0375
0306	0316	0326	0336	0346	0356	0366	0376
0307	0317	0327	0337	0347	0357	0367	0377

No. 4
(with D I/O selected)



0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0400 ~ 0407	0440 ~ 0447	0500 ~ 0507	0540 ~ 0547	0600 ~ 0607	0640 ~ 0647	0700 ~ 0707	0740 ~ 0747
0410 ~ 0417	0450 ~ 0457	0510 ~ 0517	0550 ~ 0557	0610 ~ 0617	0650 ~ 0657	0710 ~ 0717	0750 ~ 0757
0420 ~ 0427	0460 ~ 0467	0520 ~ 0527	0560 ~ 0567	0620 ~ 0627	0660 ~ 0667	0720 ~ 0727	0760 ~ 0767
0430 ~ 0437	0470 ~ 0477	0530 ~ 0537	0570 ~ 0577	0630 ~ 0637	0670 ~ 0677	0730 ~ 0737	0770 ~ 0777

NOTE: The respective expansion I/O racks containing C I/O and D I/O units may be connected in any order to the CPU rack or expansion I/O rack in the preceding stage.

4. For each of the CPU rack and expansion I/O racks, it is required to specify whether C I/O units or D I/O units are used, by means of the C I/O, D I/O selector switch.

- **C I/O, D I/O selector switch on CPU rack**

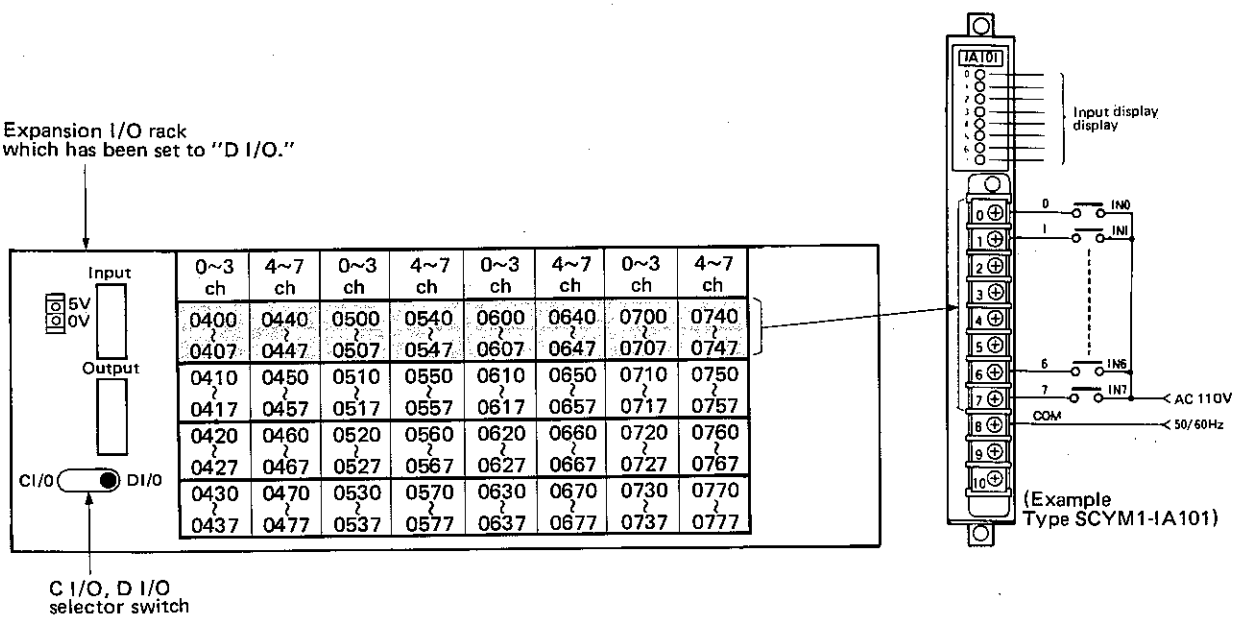
C I/O selection:
Set the selector switch to the "C I/O" position when C I/O units are used in the I/O unit section of the CPU rack. I/O relay numbers are automatically assigned to 0000 to 0077 (64 points).
D I/O selection:
Set the selector switch to the "D I/O" position when D I/O units are used in the I/O unit section of the CPU rack. I/O relay numbers are automatically assigned to 0000 to 0377 (256 points).
OFF selection:
Set the selector switch to the "OFF" position when the I/O unit section of the CPU rack is not used. I/O relay numbers will not be assigned and the I/O relay numbers of the expansion I/O rack which is connected next to the CPU rack will start from "0000."

C I/O, D I/O selector switch on each expansion I/O rack

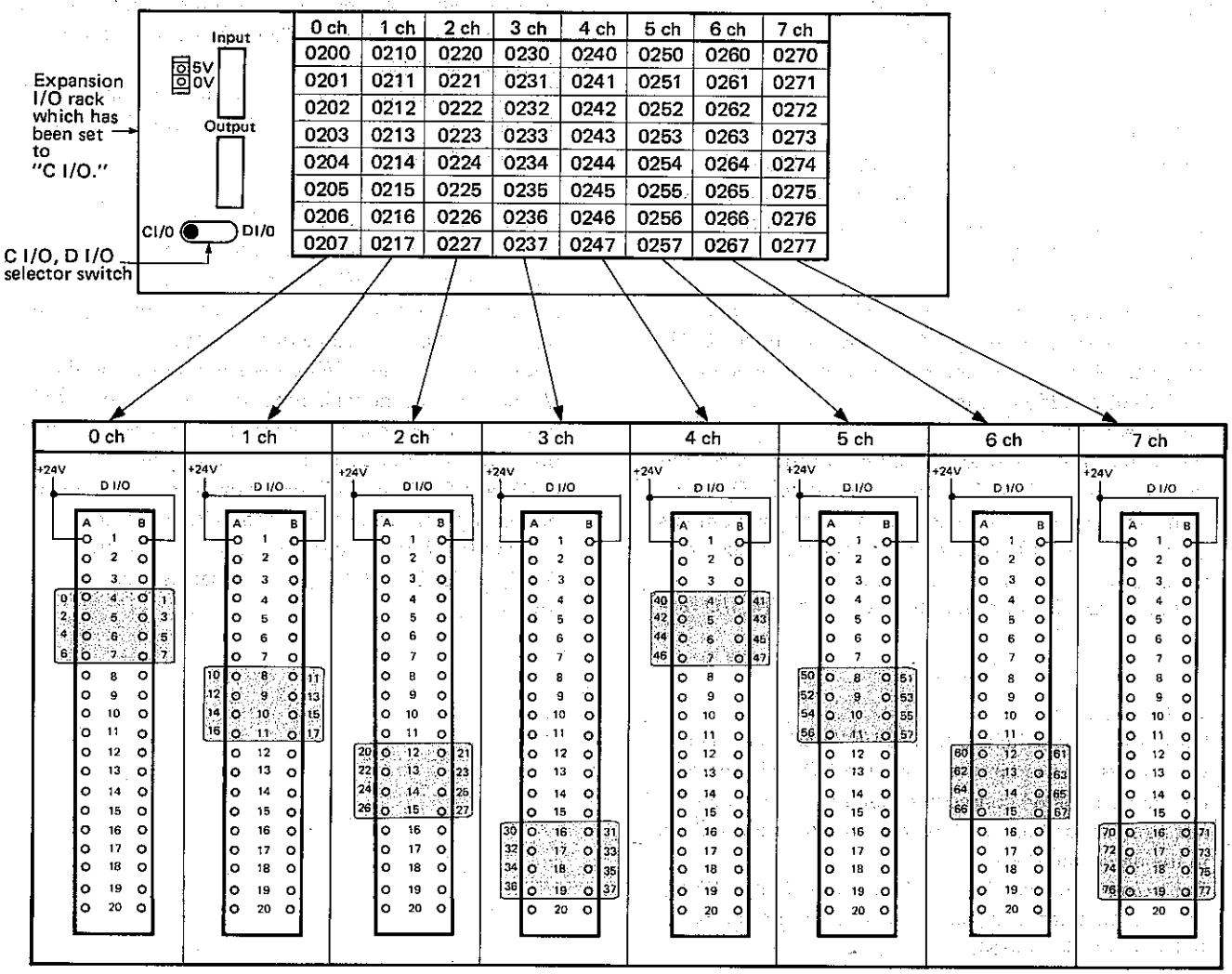
C I/O selection:
Set the selector switch to the "C I/O" position when C I/O units are used in the expansion I/O rack. I/O relay numbers will be 64 consecutive numbers following the last number used for the CPU rack or expansion I/O rack in the preceding stage.
For example, if the relay numbers are used up to 0177, the relay numbers assigned to the C I/O units are 0200 to 0277 (for 64 points).

D I/O selection:
Set the selector switch to the "D I/O" position when D I/O units are used in the expansion I/O rack. I/O relay numbers will be 256 consecutive numbers following the last number used for the CPU rack or expansion I/O rack in the preceding stage.
For example, if the relay numbers are used up to 0177, the relay numbers assigned to the D I/O units are 0200 to 0577 (for 256 points).

5. If C I/O units are mounted in the CPU rack and expansion I/O rack which have been set to "D I/O", only the 8 points of the I/O relay numbers at the top of the D I/O base unit will operate. The remaining 24 points may be used as internal auxiliary relays.
For example, when C I/O units are mounted on the D I/O base unit as shown below, I/O relay numbers will operate as 0400 to 0407, 0440 to 0447, 0500 to 0507, 0540 to 0547, 0600 to 0607, 0640 to 0647, 0700 to 0707, and 0740 to 0747, respectively and the remaining numbers 0410 to 0437, 0450 to 0477, 0510 to 0537, 0550 to 0577, 0610 to 0637, 0650 to 0677, 0710 to 0737, and 0750 to 0777 may be used as internal auxiliary relays.



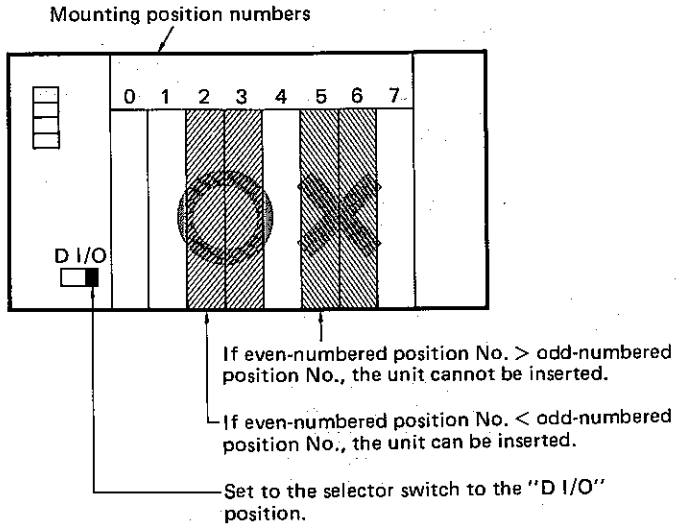
6. When D I/O units are mounted in the CPU rack or expansion I/O rack which has been set to "C I/O", I/O relay numbers will be as shown below.



0 ch	1 ch	2 ch	3 ch	4 ch	5 ch	6 ch	7 ch
0200	0210	0220	0230	0240	0250	0260	0270
0201	0211	0221	0231	0241	0251	0261	0271
0202	0212	0222	0232	0242	0252	0262	0272
0203	0213	0223	0233	0243	0253	0263	0273
0204	0214	0224	0234	0244	0254	0264	0274
0205	0215	0225	0235	0245	0255	0265	0275
0206	0216	0226	0236	0246	0256	0266	0276
0207	0217	0227	0237	0247	0257	0267	0277

NOTE: In the above figure, the D I/O terminals enclosed in a box ( ) must be wired for each channel.

7. When high-speed counter I/O units are to be mounted on the CPU rack or expansion I/O rack, set the C I/O, D I/O selector switch to the "D I/O" position. One high-speed counter I/O unit requires a mounting space for 2 D I/O units (i.e., for 8 channels).
When mounting the high-speed counter I/O units, use mounting positions only in the following combinations: Mounting position numbers 0 and 1, 2 and 3, 4 and 5, or 6 and 7. For example, the combination of mounting position numbers 5 and 6 cannot be used.

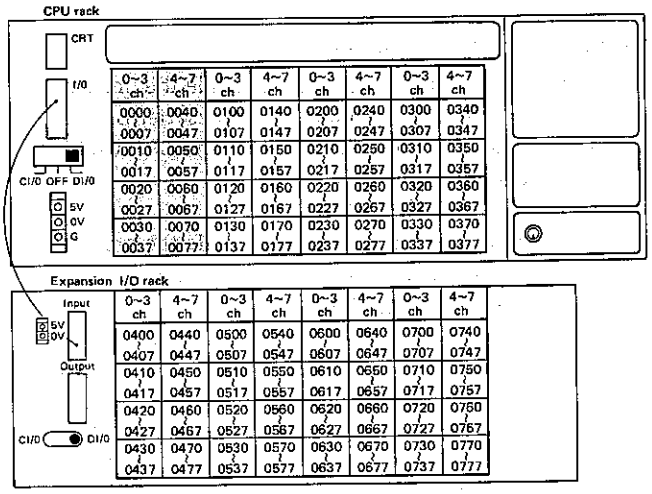


Address			Signal name		Address			Signal name	
Channel		Bit			Channel		Bit		
XX	0	0	1	×10⁰	XX	4	0	1	×10⁰
		1	2				1	2	
		2	4				2	4	
		3	8				3	8	
		4	1	×10¹			4	1	×10¹
		5	2				5	2	
		6	4				6	4	
		7	8				7	8	
	1	0	1	×10²		5	0	1	×10²
		1	2				1	2	
		2	4				2	4	
		3	8				3	8	
		4	1	×10³			4	1	×10³
		5	2				5	2	
		6	4				6	4	
		7	8				7	8	
	2	0	1	×10⁴		6	0	1	×10⁴
		1	2				1	2	
		2	4				2	4	
		3	8				3	8	
		4	1	×10⁵			4	1	×10⁵
		5	2				5	2	
		6	4				6	4	
		7	8				7	8	
	3	0	A coincidence flag clear			7	0	A coincidence flag	
		1	A preset				1	A=	
		2	Reset				2	A>	
		3	B coincidence flag clear				3	B coincidence flag	
		4	B preset				4	B=	
		5	(Not used)				5	B>	
		6	(Not used)				6	Normally ON	
		7	(Not used)				7	Normally ON	

Preset value

Current value

NOTES:
1. For example, when a high-speed counter I/O unit is mounted in the positions marked ▭ on the CPU rack, the digits "xx" indicated in NOTE 2 below will become "00".
2. Channels xx0 to xx3 are for output, while channels xx4 to xx7 are for input.

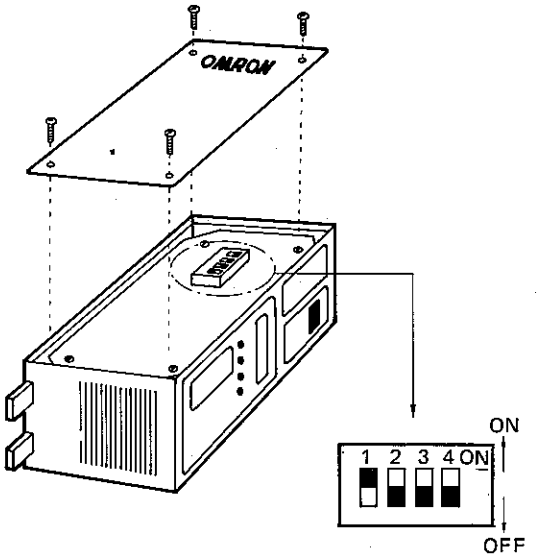


- **Signal description**
- Set value (xx00 to xx27) (CPU to CNT20)
  This signal serves as data to be preset in the presetter whichever "A preset (xx31)" or "B preset (xx34)" is ON.
- A preset (xx31) (CPU to CNT20)
  After this signal is turned ON at the preset gate of presetter A, a set value is transferred. This signal turns OFF after the transfer of the set value.
- B preset (xx34) (CPU to CNT20)
  After this signal is turned OFF at the preset gate of presetter B, a set value is transferred. This signal turns OFF after the transfer of the set value.
- A coincidence flag clear (xx30) (CPU to CNT20)
  A coincidence flag is cleared when this signal is turned ON.
- B coincidence flag clear (xx33) (CPU to CNT20)
  B coincidence flag is cleared when this signal is turned ON.
- Reset (xx32) (CPU to CNT20)
  The counter and A and B coincidence flags are being reset while this signal is ON. (This signal is ORed with external reset input signal RES.)
- Current value (xx40 to xx67) (CNT20 to CPU)
  This signal represents the present count value. This data is always fetched into the CPU starting from the least significant digit.
  An error may result if the data is fetched starting from the most significant digit.
- A coincidence flag (xx70) (CNT20 to CPU)
  This flag is set when the present count value coincides with the value of presetter A. This flag is reset by A coincidence flag clear signal or Reset signal.
- B coincidence flag (xx73) (CNT20 to CPU)
  This flag is set when the present count value coincides with the value of presetter B. This flag is reset by B coincidence flag clear signal or Reset signal.
- A= (xx71) (CNT20 to CPU)
  This signal is continuously output while the present count value is equal to the value of presetter A. (This signal may not be fetched into the CPU while counting at high speeds.)
- B= (xx74) (CNT20 to CPU)
  This signal is continuously output while the present count value is equal to the value of presetter B. (This signal may not be fetched into the CPU while counting at high speeds.)
- A> (xx72) (CNT20 to CPU)
  This signal is continuously output while the present count value is greater than the value of presetter A.
- B> (xx75) (CNT20 to CPU)
  This signal is continuously output while the present count value is greater than the value of presetter B.
- CP1 Input (See NOTES below.)
  This signal is used as a count input signal in command input mode. In phase differential input mode, this signal becomes an input 90° advanced in phase to CP2 in up counting.
- CP2 Input (See NOTES below.)
  This signal is used as up (add)/down (subtract) mode select signal in command input mode.
- RES input
  An input signal to reset the counter and A and B coincidence flags.

NOTES: 1. DIP switch setting
The 4-pin DIP switch must be set as follows according to the input mode of CP1 or CP2.

DIP switch / Input mode	Pin No. 1	2	3	4
Phase differential	ON	OFF	OFF	OFF
Command	OFF	ON	OFF	OFF

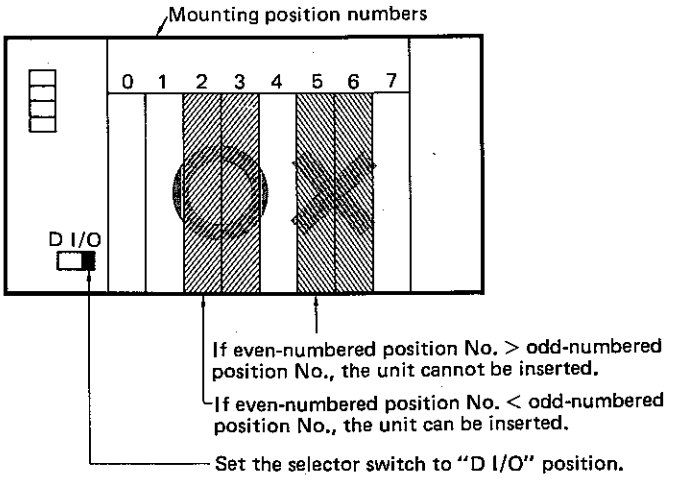
2. DIP switch location



(Setting for phase differential input mode)

3. Shielded cable should be used for input signals.

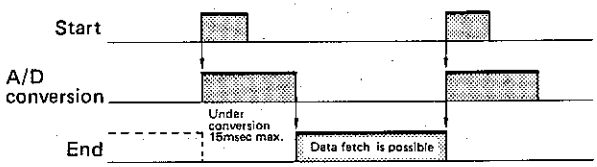
8. When A/D conversion units are to be mounted on the CPU rack or expansion I/O rack, set the C I/O, D I/O selector switch to the "D I/O" position. One A/D conversion unit requires a mounting space for 2 D I/O units (i.e., for 8 channels).
When mounting the A/D conversion units, use mounting positions only in the following combinations: Mounting position numbers 0 and 1, 2 and 3, 4 and 5, or 6 and 7. For example, the combination of mounting position numbers 5 and 6 cannot be used.



IN A				IN B			
Address			Signal name	Address			Signal name
Channel		Bit		Channel		Bit	
XX	0	0	1	XX	4	0	1
		1	2			1	2
		2	4 (x10⁰)			2	4 (x10⁰)
		3	8			3	8
		4	1			4	1
		5	2			5	2
		6	4 (x10¹)			6	4 (x10¹)
		7	8			7	8
	1	0	1		5	0	1
		1	2			1	2
		2	4 (x10²)			2	4 (x10²)
		3	8			3	8
		4	Over A			4	Over B
		5				5	
		6				6	
		7				7	
	2	0	End A		6	0	End B
		1				1	
		2				2	
		3				3	
		4	Not used.			4	Not used.
		5				5	
		6				6	
		7				7	
	3	0	Start A		7	0	Start B
		1				1	
		2				2	
		3				3	
		4	Not used.			4	Not used.
		5				5	
		6				6	
		7				7	

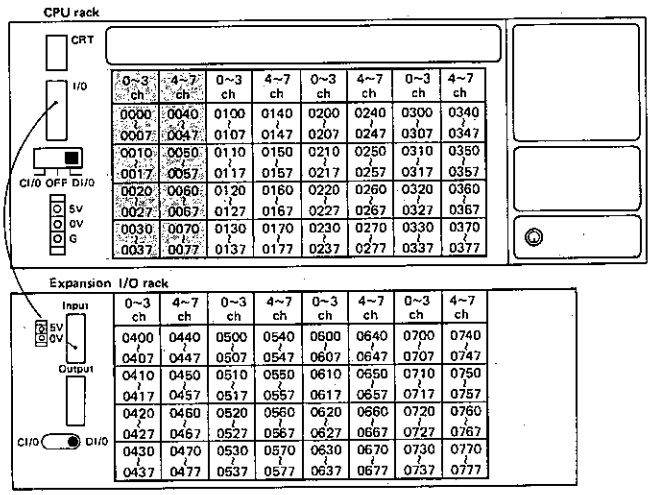
(Digital data A: IN A, channels 0 and 1; Digital data B: IN B, channels 4 and 5)

- **Signal description**
- Digital Data A and B
  These signals are 3-digit BCD signals from A/D converters A and B, respectively.
  Either signal is in the latched state after the output of End A or B signal until the next Start A or B signal is applied.
- Start A and B
  These signals are used to start A/D converters A and B, respectively.
- End A and B
  These signals indicate the end of operation by the respective A/D converters. Digital data A or B is fetched into the CPU after confirming End A or B signal. Either signal is reset by the next Start A or B signal.

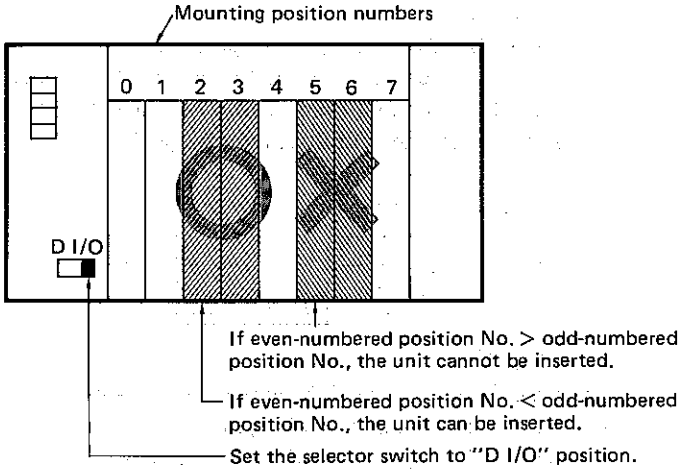


- Over A and B
  Over A or B signal is set if the voltage or current input exceeds 5V or 20mA, respectively. Linearity is not compensated at inputs exceeding these values.

NOTES:
1. For example, when an A/D conversion unit is mounted in the positions marked [ ] on the CPU rack, the digits "xx" indicated in NOTE 2 below will become "00".
2. Channels xx0 to xx3 are for IN A, while channels xx4 to xx7 are for IN B.



9. When D/A conversion units are to be mounted on the CPU rack or expansion I/O rack, set the C I/O, D I/O selector switch to the "D I/O" position. One D/A conversion unit requires a mounting space for 2 D I/O units (i.e., for 8 channels).
When mounting D/A conversion units, use mounting positions only in the following combinations: Mounting position numbers 0 and 1, 2 and 3, 4 and 5, or 6 and 7. For example, the combination of mounting position numbers 5 and 6 cannot be used.



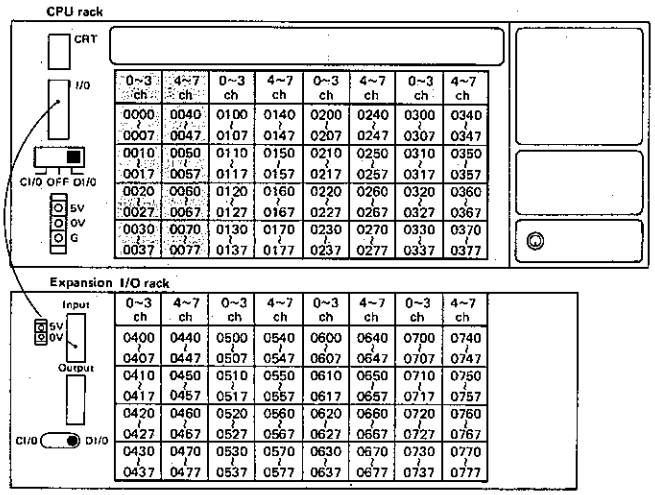
- **Signal description**
- Digital Data A, B
  This is a 3-digit BCD signal for D/A conversion. Output of each digit must always start with a low-order digit. If the digit output sequence is reversed, correct data output cannot be guaranteed.

Out A				Out B			
Address			Signal name	Address			Signal name
Channel		Bit		Channel		Bit	
XX	0	0	1	XX	4	0	1
		1	2			1	2
		2	4 ×10⁰			2	4 ×10⁰
		3	8			3	8
		4	1			4	1
		5	2			5	2
		6	4 ×10¹			6	4 ×10¹
		7	8			7	8
	1	0	1		5	0	1
		1	2			1	2
		2	4 ×10²			2	4 ×10²
		3	8			3	8
		4				4	
		5				5	
		6				6	
		7				7	
	2	0	End A		6	0	End B
		1				1	
		2				2	
		3				3	
		4	Not used.			4	Not used.
		5				5	
		6				6	
		7				7	
	3	0	Start A		7	0	Start B
		1				1	
		2				2	
		3				3	
		4	Not used.			4	Not used.
		5				5	
		6				6	
		7				7	

Digital data A

Digital data B

NOTES:
1. For example, when a D/A conversion unit is mounted in the positions marked [ ] on the CPU rack, the digits "xx" indicated in NOTE 2 below will become "00".
2. Channels xx0 to xx3 are for IN A, while channels xx4 to xx7 are for IN B.



3.3 Determination of Internal Auxiliary Relay Numbers

The SYSMAC-M1R has 224 internal auxiliary relays which are used for internal data transfer in sequence circuits. They are independent of I/O devices in sequence. Since the internal auxiliary relays are the data memories incorporated in the CPU, no I/O unit is required to be mounted.

- Relay numbers 1000 to 1337 may not necessarily be assigned consecutively.
- Relay coil numbers cannot be used in duplication within the same program. However, the number of relay contacts is not limited for use.
- If more than 224 internal auxiliary relays are required, I/O relay numbers to which no I/O unit is connected may be used. When an output unit to which no output device is connected is mounted, its output relay numbers may also be used as internal auxiliary relays.

3.4 Determination of Special Auxiliary Relay Numbers

28 special auxiliary relays are provided. These relays are sort of internal auxiliary relays which operate and release according to the internal conditions controlled by hardware and are independent of the I/O devices in sequence.

Relay Nos. 1340 to 1347:

The FAL No. (00 to 99) when the Diagnostic (FAL) instruction is executed is output in BCD to each of relay numbers 1340 to 1347. If these relays are to be reset, executed the FAL00 instruction and the logical state of all the relays becomes "0."

1347	1346	1345	1344	1343	1342	1341	1340
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
$\times 10^1$ High-order digits				$\times 10^0$ Low-order digits			

Relay Nos. 1350 to 1357:

These relays output the calculation result when Add (+) or Subtract (—) instruction is executed, in BCD to each of relay numbers 1350 to 1357. The output status of each relay is held until the next arithmetic operation instruction is executed.

1357	1356	1355	1354	1353	1352	1351	1350
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
$X10^1$ High-order digits				$X10^0$ Low-order digits			

Relay No. 1360:

This relay operates (ON) if a carry exists in the result when the Add (+) instruction is executed. This relay also operates if a borrow exists in the result when the Subtract (—) instruction is executed. When the next arithmetic operation instruction is executed, the logical state of the relay changes. The relay releases (OFF) when the END instruction is executed.

Relay Nos. 1361 to 1363:

These relays output the result when the Compare (CMP) instruction is executed.

Relay No. 1361 operates if the result is less than (<).

Relay No. 1362 operates when the result is equal (=).

Relay No. 1363 operates when the result is more than (>).

The logical state of each relay changes when the next Compare instruction is executed. These relays release when the END instruction is executed.

Relay Nos. 1364 and 1366:

These relays are normally in the OFF state.

Relay Nos. 1365 and 1367:

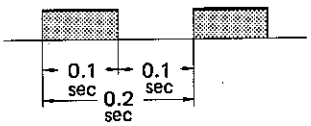
These relays are normally in the ON state.

Relay No. 1374:

This relay operates when a battery failure occurs and releases when the battery is returned to normal. When this relay operates, the ERROR indicator on the front panel of the CPU illuminates. If the BAT FAULT signal is desired to be transmitted externally, prepare and program a circuit using the contacts of this relay.

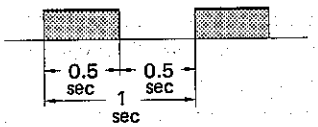
Relay No. 1375:

This relay is used to generate 0.2sec clock. When used in combination with a counter, it functions as a timer for memory retention during a power failure and as a long-time timer.



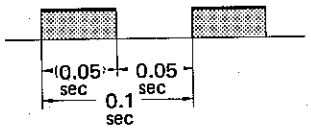
Relay No. 1376:

This relay is used to generate 1sec clock. When used in combination with a counter, it functions as a timer for memory retention during a power failure and as a long-time timer. The relay output can also be used as a flicker signal.



Relay No. 1377:

This relay is used to generate 0.1 sec clock. When used in combination with a counter, it functions as a timer for memory retention during a power failure.

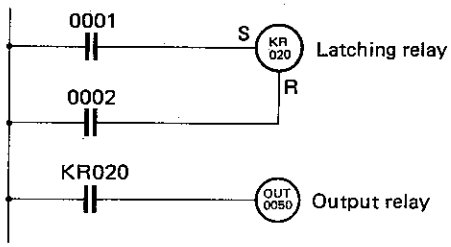


NOTES:
1. The ON time of 0.1sec clock is 50msec. Therefore, note that if the program execution time is prolonged, the CPU may fail to read the clock.
2. If the program capacity exceeds 2k words, be sure to use 0.2sec clock.

3.5 Determination of Latching Relay Numbers

The SYSMAC-M1R has 256 latching relays whose operating states before a power failure can be retained in the memory. Since the operating states of these relays are stored in the memory, all their outputs at the time of the power failure are turned off, but the relays will return to the state before the power failure when power is applied again.

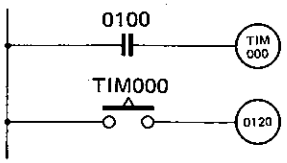
- Relay numbers 000 ~ 377 may not necessarily be assigned consecutively.
- When using a latching relay, the letters "KR" must be prefixed to the relay number. (ex. KR020)
- Relay coil numbers cannot be used in duplication. However, the number of relay contacts is not limited.
- When set and reset input signals are applied simultaneously, the reset input signal takes precedence over the set input signal.
- These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay.



3.6 Determination of Timer/Counter Numbers

The SYSMAC-M1R has 128 timers and counters which are used for timer/counter numbers in programming.

- Timer/counter numbers 000 ~ 177 are shared by both timers and counters. Therefore, a number already assigned to a timer cannot be used for any other counter.
- The same number will be used for both the coil and contact numbers of a timer or counter. To distinguish timer/counter contact numbers from input relay numbers, shift register and latching relay numbers, the letters "TIM" or "CNT" must be prefixed to each timer/counter contact number (e.g., TIM000, CNT001).



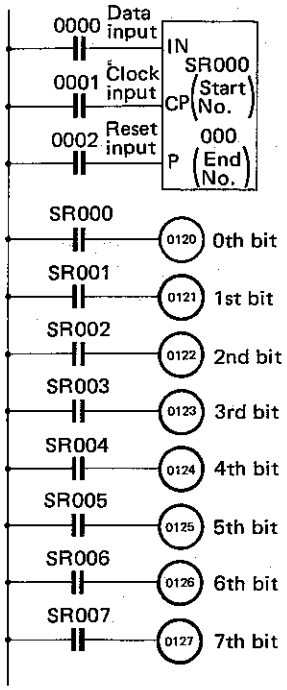
3.7 Determination of Temporary Memory Relay Numbers

The SYSMAC-M1R has 8 temporary memory relays which are used when plural outputs exist in a block.

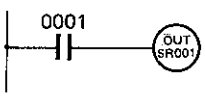
- Relay numbers 0 ~ 7 may not necessarily be assigned consecutively.
- Temporary memory relay coil numbers cannot be used in duplication within the same block. With two or more blocks, they can be used in duplication.
- When using a temporary memory relay, the letters "TR" must be prefixed to the relay number (e.g., TR0).

3.8 Determination of Shift Register Numbers

The SYSMAC-M1R has 32 shift registers (each consisting of 8 bits). With SR (Shift Register) instructions, the low-order digit always becomes "0" (000, 010, 020, 030, 040, 050, 060, 070, 100, 110, 120, 130, 140, 150, 160, 170, 200, 210, 220, 230, 240, 250, 260, 270, 300, 310, 320, 330, 340, 350, 360, 370). These instructions can be increased or decreased in units of 8 bits. The low-order digit of each bit becomes 0 ~ 7.



- Relay numbers 000 ~ 370 may not necessarily be assigned consecutively.
- Be sure to satisfy the condition; Start No. ≤ End No.
- Shift register coil numbers cannot be used in duplication. However, the number of contacts is not limited.
- When set and reset input signals are applied simultaneously, the reset input signal takes precedence over the set input signal.
- The shift register outputs cannot be transmitted directly to an output terminal. If any of the outputs is desired to be transmitted externally, prepare and program a circuit so that the output is transmitted externally through an output relay.
- Shift registers can also be used as auxiliary relays when used with an OUT instruction.



- When using a shift register, the letters "SR" must be prefixed to the relay number (e.g., SR001).

4. Instruction Words

4.1 List of Instructions

No.	Instruction	Symbol	Function	Word length	Data
1	LOAD	LD	Logical start operation.	1W	Input/output relays 0000~0777 Internal auxiliary relays 1000~1337 Special auxiliary relays 1340~1367 1374~1377 Timers/counters 000~ 177 Latching relays 000~ 377 Shift registers 000~ 377 Temporary memory relays 0~ 7 (Only LOAD instruction can be used for temporary memory relays.)
2	LOAD NOT	LD NOT	Logical NOT start operation.	1W	
3	AND	AND	Logical AND operation.	1W	
4	AND NOT	AND NOT	Logical AND NOT operation.	1W	
5	OR	OR	Logical OR operation.	1W	
6	OR NOT	OR NOT	Logical OR NOT operation.	1W	
7	AND LOAD	AND LD	Logical AND operation with the previous condition.	1W	–
8	OR LOAD	OR LD	Logical OR operation with the previous condition.	1W	
9	OUT	OUT	Outputs the result of a logical operation to the specified output relay, internal auxiliary relay, latching relay or shift register.	1W	Input/output relays 0000~0777 Internal auxiliary relays 1000~1337 Latching relays 1360 Shift registers 000~ 377 Temporary memory relays 0~ 7 (Only OUT instruction can be used for temporary memory relays.)
10	OUT NOT	OUT NOT	Inverts the results of a logical operation and then outputs them to the specified output relay, internal auxiliary relay, latching relay or shift register.	1W	
11	TIMER	TIM	On-delay timer operation.	2W	Timers/counters 000~ 177
12	COUNTER	CNT	Down counter operation.	2W	
13	LATCHING RELAY	KR	Latching relay operation.	1W	Latching relays 000~ 377
14	SHIFT REGISTER	SR	Shift register operation.	2W	Shift registers 000~ 377
15	INTERLOCK	FUNC IL	Causes all the relay coils between this instruction and the ILC instruction to be reset or not reset according to the result immediately before this instruction.	1W	–
16	INTERLOCK CLEAR	FUNC ILC	Clears the IL instruction.	1W	
17	JUMP	FUNC JMP	Causes all the contents of a program between this instruction and the JME instruction to be ignored or executed according to the result immediately before this instruction.	1W	
18	JUMP END	FUNC JME	Clears the JMP instruction.	1W	
19	MOVE (MOV)	FUNC MOV	Transfers data between I/Os.	2W	1st word: 000~137, KR00~37, SR 00~99, ※00~※99 2nd word: 000~133, KR00~37, SR 00~37 TIM, CTN 000~177: 000~132, KR00~36, SR 00~36
20	MOVE NOT (MOV NOT)	FUNC MOV NOT	Inverts and transfers data between I/Os.	2W	

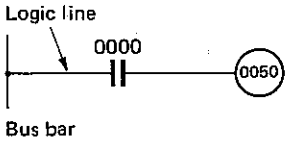
No.	Instruction	Symbol	Function	Word length	Data
21	COMPARE (CMP)	FUNC CMP	Compares data between I/Os.	2W	1st word: 000~135, KR00~37, SR 00~37, ※00~※99 2nd word: 000~135, KR00~37, SR 00~37
22	ADD (ADD)	FUNC +	Adds data between I/Os.	2W	1st word: 000~134, KR00~37, SR 00~37, ※00~※99 2nd word: 000~134, KR00~37, SR 00~37
23	SUBTRACT (SUB)	FUNC −	Subtracts data between I/Os.	2W	
24	DIAGNOSTIC (FAL)	FUNC FAL	Indicates the type of failure or abnormal mode.	1W	00~99
25	END	FUNC END	The end of a program.	1W	–

CAUTION:
The FUNC key must be first depressed before executing any of the instructions numbered 15 through 25 in the above list.

4.2 Explanation of Instruction Words

■ LOAD (LD) & OUTPUT (OUT) INSTRUCTIONS

If each logic line starts with an NO contact, use the LD instruction. Use the OUT instruction for a relay coil.



Coding

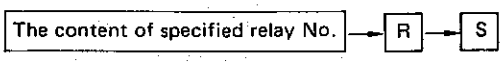
Address	OP	Data
0000	LD	0000
0001	OUT	0050

Contents of Registers

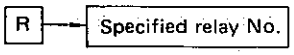
R	S
0000	—
0000	—

- **Operation of each register**

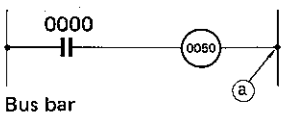
The LD instruction causes the content (ON or OFF state) of the specified relay number to be stored into the RESULT REGISTER (hereafter referred to as "R register"). It also causes the previous result in the R register to be transferred to the STACK REGISTER (hereafter referred to as "S register").



The OUT instruction causes the content of the R register to be output to the specified relay number. In this case, the content of the R register will remain unchanged.



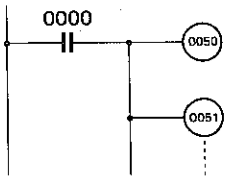
- Bus bar of a different phase is not required to be programmed.



Connection to the bus bar of a different phase (part ⓐ) is accomplished automatically by programming an OUT instruction.

- **Consecutive OUT instructions**

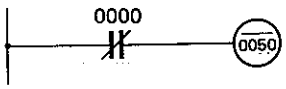
If the OUT instruction is followed by another OUT instruction, this condition is regarded as a circuit error during the program check. However, each output relay operates normally.



OP	Data
LD	0000
OUT	0050
OUT	0051
⋮	⋮

■ LOAD NOT (LD·NOT) & OUTPUT NOT (OUT·NOT) INSTRUCTIONS

If each logic line starts with an NC contact, use the LD·NOT instruction in place of the LD instruction. Use the OUT·NOT instruction to invert the output condition.



Coding

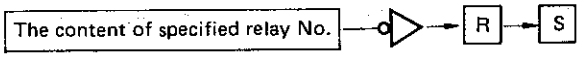
Address	OP	Data
0000	LD·NOT	0000
0001	OUT·NOT	0050

Contents of Registers

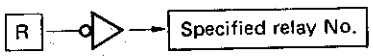
R	S
0000	—
0000	—

- **Operation of each register**

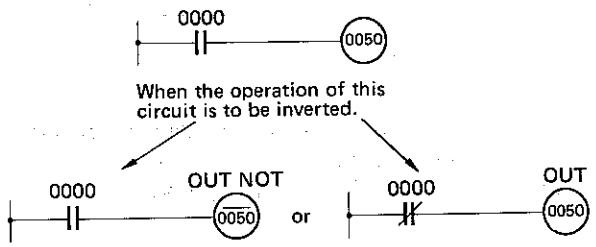
The LD·NOT instruction causes the content of the specified relay number to be inverted and then stored into the R register.



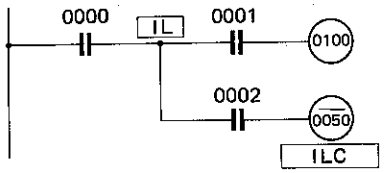
The OUT·NOT instruction causes the content of the R register to be inverted and then output to the specified relay number. In this case, the content of the R register will remain unchanged.



- **Application of OUT·NOT instruction**



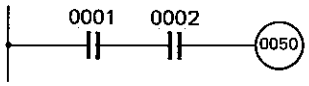
- **Use of OUT·NOT instruction between IL and ILC instructions**



Note that relay 0050 operates when the IL condition (0000) is OFF.

■ AND INSTRUCTION

NO contacts in series are processed by the AND instruction.



Coding

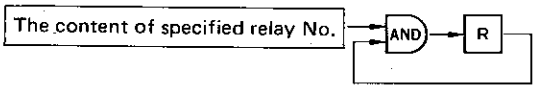
Address	OP	Data
0000	LD	0001
0001	AND	0002
0002	OUT	0050

Contents of Registers

R	S
0001	—
0001 0002	—
0001 0002	—

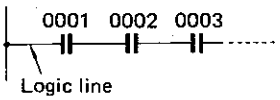
- **Operation of each register**

The AND instruction causes the logical AND operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of the AND key.

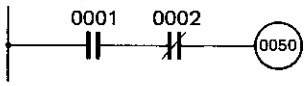


OP	Data
LD	0001
AND	0002
AND	0003
⋮	⋮

In this case, the contact of the first relay number 0001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD0001."

■ AND-NOT INSTRUCTION

If an NC contact is connected in series, use the AND-NOT instruction in place of the AND instruction.



Coding

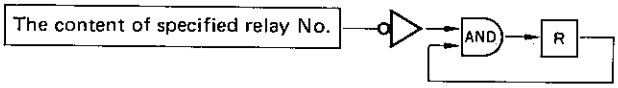
Address	OP	Data
0000	LD	0001
0001	AND-NOT	0002
0002	OUT	0050

Contents of Registers

R	S
0001	—
0001 0002	—
0001 0002	—

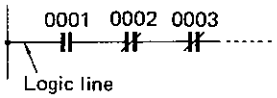
- **Operation of each register**

The AND-NOT instruction causes the content of the specified relay number to be inverted and then ANDed with the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected in series by means of AND NOT keys.

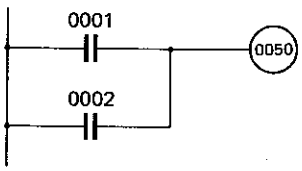


OP	Data
LD	0001
AND-NOT	0002
AND-NOT	0003
⋮	⋮

In this case, the contact of the first relay number 0001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD0001."

■ OR INSTRUCTION

NO contacts in parallel are processed by the OR instruction.



Coding

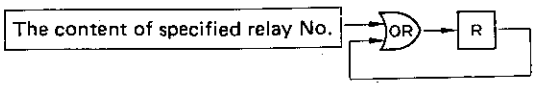
Address	OP	Data
0000	LD	0001
0001	OR	0002
0002	OUT	0050

Contents of Registers

R	S
0001	—
0001 0002	—
0001 0002	—

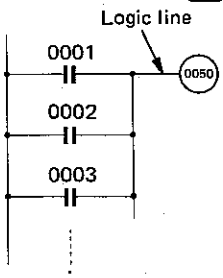
- **Operation of each register**

The OR instruction causes the logical OR operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of the [OR] key.

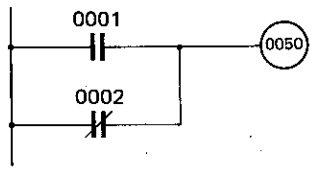


OP	Data
LD	0001
OR	0002
OR	0003
⋮	⋮
OUT	0050

In this case, the contact of the first relay number 0001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD0001."

■ OR·NOT INSTRUCTION

If an NC contact is to be connected in parallel, use the OR·NOT instruction in place of the OR instruction.



Coding

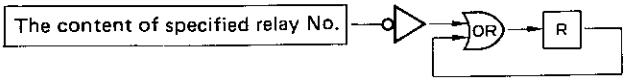
Address	OP	Data
0000	LD	0001
0001	OR·NOT	0002
0002	OUT	0050

Contents of Registers

R	S
0001	—
0001 0002	—
0001 0002	—

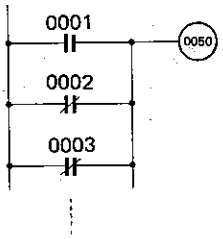
- **Operation of each register**

The OR·NOT instruction causes the content of the specified relay number to be inverted and then ORed with the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**

The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected by means of [OR] [NOT] keys.

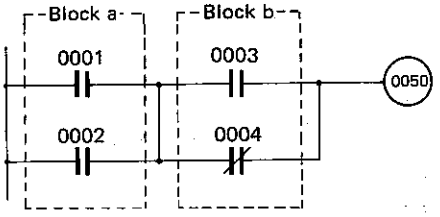


OP	Data
LD	0001
OR·NOT	0002
OR·NOT	0003
⋮	⋮
OUT	0050

In this case, the contact of the first relay number 0001 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD0001."

■ AND·LOAD (AND·LD) INSTRUCTION

For inter-block AND operation between two or more blocks, use the AND·LD instruction.



Coding

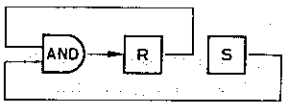
Address	OP	Data
0000	LD	0001
0001	OR	0002
0002	LD*	0003
0003	OR·NOT	0004
0004	AND·LD**	
0005	OUT	0050

Contents of Registers

R	S
0001	—
0001 0002	—
0003	0001 0002
0003 0004	0001 0002
0001 0003 0002 0004	—
0001 0003 0002 0004	—

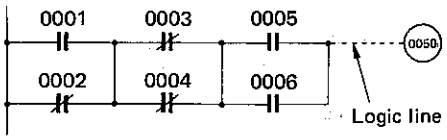
NOTES: * Use this instruction as the first instruction for the next block to be ANDed with the preceding block.
** Use the AND·LD instruction for series connection of two blocks (blocks a and b).

- **Operation of each register**
  1. By the LD0001 and OR0002 instructions, the result of the logical OR operation in block a is stored into the R register.
  2. By the LD0003 instruction in block b, the result of the operation in block a is transferred into the S register, while the result of the logical operation by instructions LD0003 and OR·NOT0004 in block b is stored into the R register.
  3. AND·LD instruction causes the logical AND operation to be performed between the R register and the S register. The result of the logical AND operation will be newly stored into the R register.



- **Number of blocks**

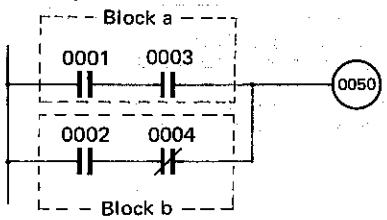
The number of blocks is not limited for AND·LD operation of a logic line. As many blocks as required can be continued for series connection by means of [LD] ~ [AND] [LD] keys.



OP	Data
LD	0001
OR·NOT	0002
LD·NOT	0003
OR·NOT	0004
AND·LD	–
LD	0005
OR	0006
AND·LD	–
⋮	⋮
OUT	0050

■ OR·LOAD (OR·LD) INSTRUCTION

For inter-block OR operation between two or more blocks, use the OR·LOAD instruction.



Coding

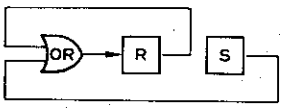
Address	OP	Data
0000	LD	0001
0001	AND	0003
0002	LD*	0002
0003	AND·NOT	0004
0004	OR·LD**	–
0005	OUT	0050

Contents of Registers

R	S
0001	—
0001 0003	—
0002	0001 0003
0002 0004	0001 0003
0001 0003 0002 0004	—
0001 0003 0002 0004	—

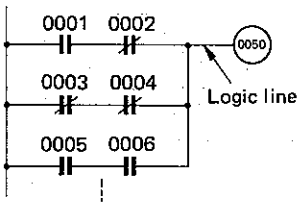
NOTES: * Use this LD instruction as the first instruction of the next block to be ORed with the preceding block.
** Use the OR·LD instruction for parallel connection of two blocks (blocks a and b).

- **Operation of each register**
  1. By the LD0001 and AND0003 instructions, the result of the logical AND operation in block a is stored into the R register.
  2. By the LD0002 instruction in block b, the result of the operation in block a is transferred into the S register, while the result of the logical operation by instructions LD0002 and AND·NOT0004 in block b is stored into the R register.
  3. The OR·LD instruction causes the logical OR operation to be performed between the R register and the S register. The result of the logical OR operation will be newly stored into the R register.



- **Number of blocks**

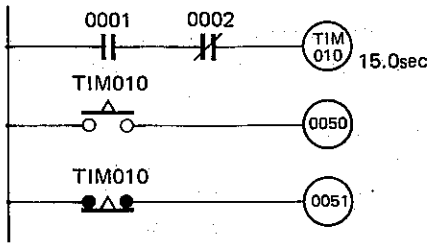
The number of blocks is not limited for OR·LD operation on a logic line. As many blocks as required can be continued for parallel connection by means of [LD] ~ [OR] [LD] keys.

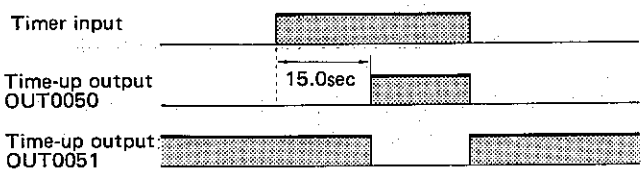


OP	Data
LD	0001
AND·NOT	0002
LD·NOT	0003
AND·NOT	0004
OR·LD	–
LD	0005
AND	0006
OR·LD	–
⋮	⋮
OUT	0050

■ TIMER (TIM) INSTRUCTION

The TIM instruction can be used as an ON-delay timer in the same manner as a relay circuit.

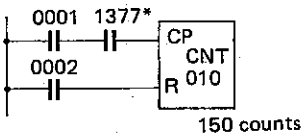




Address	OP	Data
0000	LD	0001
0001	AND-NOT	0002
0002	TIM	010*
0003		0150*
0004	LD-TIM	010
0005	OUT	0050
0006	LD-NOT-TIM	010
0007	OUT	0051

NOTES:
1. * Timer number 000 ~ 177.
2. ** Time setting value 000 ~ 999 x 0.1sec.
3. Timer numbers are shared by both timers and counters. Therefore, a number already assigned to a timer cannot be used for any other counter.

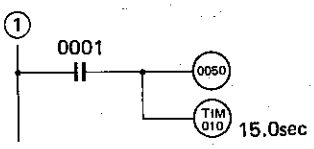
- **Operation of each register**
  The timer starts when the content of the R register is logical 1 and resets when the content of the R register is logical 0.
- **Number of contacts**
  A time-up contact designates the timer number itself. Both NO and NC contacts can be used in the required quantity.
- **Timer is of decrementing type**
  The timer is of a decrementing type which produces an output when the present value (time remaining) becomes "000." When the timer input is turned off, the present value of the timer returns to the preset value. The timer output is transmitted externally through an output relay as shown in the above circuit example.
- **Timer is reset at the time of a power failure**
  If a power failure occurs, the timer is reset and the present value returns to the preset value. Therefore, if it is required to retain the present value of the timer in the memory, a memory retentive type timer circuit as shown below must be used for programming.
- **Memory retentive type timer**
  A circuit to memorize the present value of the timer during a power failure is configured using a combination of clock instruction and counter (CNT) instruction.



OP	Data
LD	0001
AND	1377*
LD	0002
CNT	010
	150

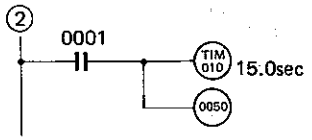
NOTE: * Special auxiliary relay 1377 is for 0.1sec clock.

- **Consecutive OUT instruction and TIM instruction**
  The operations of the circuits ① and ② below are the same, either of which may be used for programming.



OP	Data
LD	0001
OUT	0050
TIM	010
	150

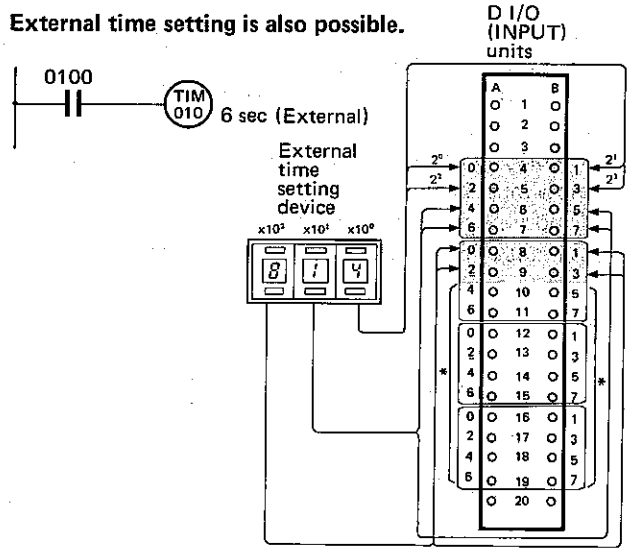
When the NO contact 0001 turns ON, output relay 0050 is energized and at the same time timer 010 starts operating.



OP	Data
LD	0001
TIM	010
	150
OUT	0050

When the NO contact 0001 turns ON, timer 010 starts operating and at the same time, output relay 0050 is energized.

- **External time setting is also possible.**

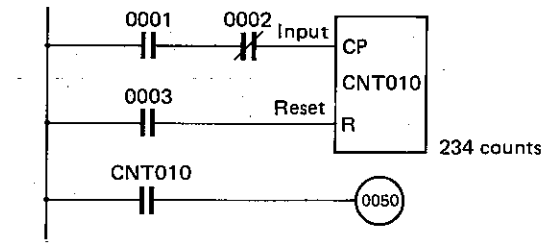


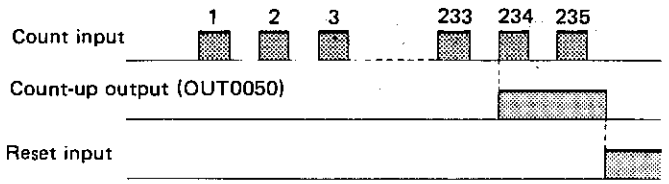
NOTE: * This area can be used for other inputs.

1. If ✳00 is specified as the second word of the data, the timer operation will be up after the lapse of 81.4sec set by the external time setting device which is connected to relay Nos. 0000 ~ 0013 as shown above.
2. For ✳□□ designation, ✳00 to ✳76 can be used.
   ✳00 → Relay Nos. 0000 ~ 0013
   ✳01 → Relay Nos. 0010 ~ 0023
   ⌇ ⌇
   ✳76 → Relay Nos. 0760 ~ 0773
3. In the above example, C I/O (input) units are used. D I/O (input) units can also be used in the same way.

■ COUNTER (CNT) INSTRUCTION

The CNT instruction can be used as a preset counter in the same manner as a relay circuit.



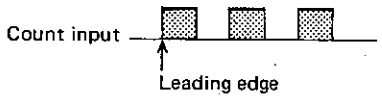


Coding

Address	OP	Data
0000	LD	0001
0001	AND·NOT	0002
0002	LD	0003
0003	CNT	010
0004		234
0005	LD·CNT	010
0006	OUT	0050

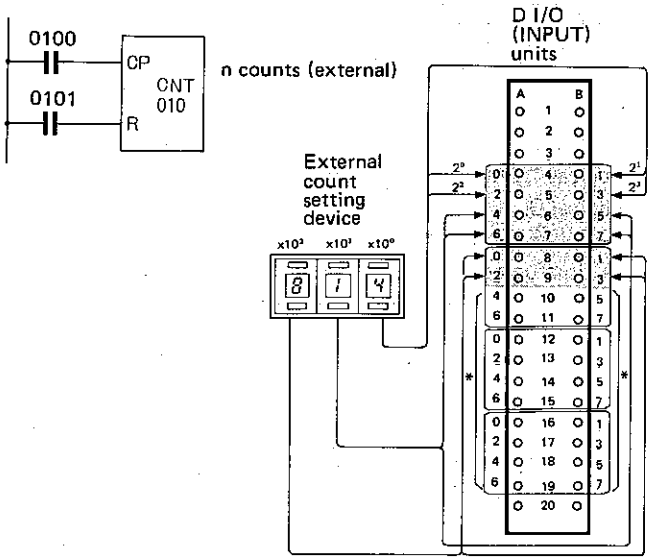
NOTES:
1. A counter program must be entered in the order of a count input circuit, a reset input circuit and a counter coil.
2. Counter number 000 ~ 177.
3. Counter setting value 000 ~ 999.
4. Counter numbers are shared by both counters and timers. Therefore, a number already assigned to a counter cannot be used for any timer.

- **Operation of each register**
  The counter resets when the content of the R register is logical 1 and is enabled to count when the content of the R register is logical 0. A count input is provided from the S register.
- **Number of contacts**
  A count-up contact designates the counter number itself. Both NO and NC contacts can be used in the required quantity.
- **Counter is of decrementing type**
  The counter is of a decrementing type which produces an output when the count value becomes "000." The present value of the counter returns to the preset value when a reset input is applied. The counter output is transmitted externally through an output relay as shown in the circuit example.
- After the preset count is up, subsequent count inputs are ignored.
- At the leading edge (i.e., from OFF to ON) of a count input signal, the counter decrements the count value by 1.



- When both a count input and a reset input are applied simultaneously, the reset input takes precedence over the count input. Even if the reset input is removed after this, the counter performs no counting operation.
- **The present value of the counter is retained in memory during a power failure**
  If a power failure occurs, the counter is not reset and the present value (i.e., count remaining) of the counter is retained in the memory.

- **External count setting is also possible.**

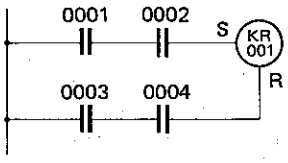


NOTE: * This area can be used for other inputs.

1. If ⁂00 is specified as the second word of the data, the counter operation will be up upon counting the value (814 counts) set by the external count setting device which is connected to the relay Nos. 0000 ~ 0013 as shown above.
2. For ⁂□□ designation, ⁂00 to ⁂76 can be used.
   ⁂00 → Relay Nos. 0000 ~ 0013.
   ⁂01 → Relay Nos. 0010 ~ 0023
   ≀ ≀
   ⁂76 → Relay Nos. 0760 ~ 0773
3. In the above example, C I/O (input) units are used, D I/O (input) units can also be used in the same way.

■ LATCHING RELAY (KR) INSTRUCTION

The KR instruction can be used as a latching relay in the same manner as a relay circuit.



Coding

Address	OP	Data
0000	LD	0001
0001	AND	0002
0002	LD	0003
0003	AND	0004
0004	KR*	001

Contents of Registers

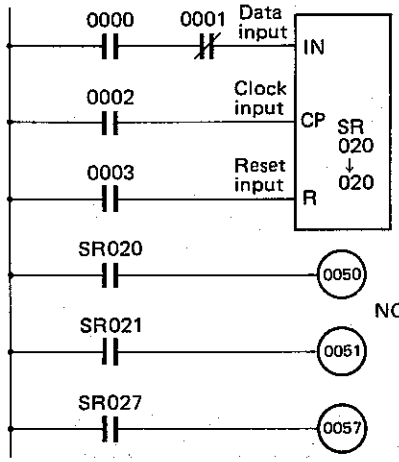
R	S
0001	—
0001 0002	—
0003	0001 0002
0003 0004	0001 0002
0003 0004	0001 0002

NOTES: * A latching relay program must be entered in the order of a set input circuit, a reset input circuit and a latching relay coil. Use the KR instruction to program a latching relay coil.

- **Operation of each register**
  The latching relay operates when the content of the R register is logical 0 and the content of the S register is logical 1. The relay releases when the content of the R register is logical 1.
- When both a set input and a reset input are applied simultaneously, the reset input takes precedence over the set input.
- The content of the latching relay is retained in the memory during a power failure. It continues to be retained until application of a reset input.

■ SHIFT REGISTER (SR) INSTRUCTION

The SR instruction can be used as a serial input shift register.

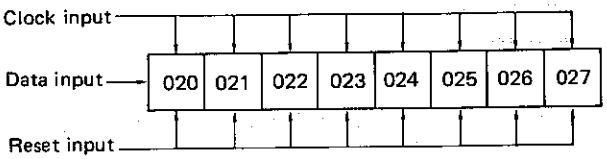


NOTE: A shift register must be programmed in the order of data input, clock input, reset input and SR.

Coding

Address	OP	Data
0200	LD	0000
0201	AND-NOT	0001
0202	LD	0002
0203	LD	0003
0204	SR	020
0205		020
0206	LD·SR	020
0207	OUT	0050
0208	LD·SR	021
0209	OUT	0051
0210	LD·SR	027
0211	OUT	0057

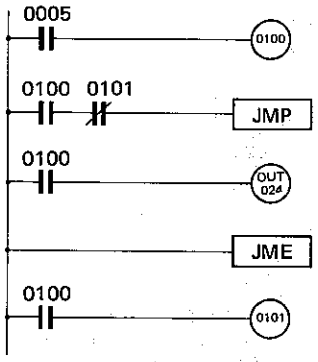
- Each SR instruction must be specified in units of 8 bits. In the above example, 8 bits from SR020 to SR027 are transferred.



- The 8-bit contents of the shift register (SR020 ~ SR027 in the above example) can be output bit by bit using a LD·SR instruction.

- When a reset input is applied to the shift register, 8 bits are reset all together.

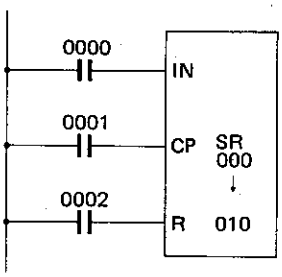
- Any of the 8 bits can be set or reset by force.



OP	Data
LD	0005
OUT	0100
LD	0100
AND-NOT	0101
JMP	
LD	0100
OUT-SR	024
JME	
LD	0100
OUT	0101

With a circuit arranged as shown above, a bit in SR024 can be set forcedly when NO contact 0005 is turned on. To reset the bit in SR024, use an OUT-NOT-SR instruction.

- Shift register exceeding 8 bits. In this case, a shift register circuit can be configured by combining two or more stages of 8-bit shift registers.

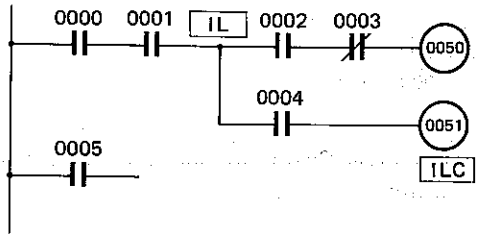


Address	OP	Data
0200	LD	0000
0201	LD	0001
0202	LD	0002
0203	SR	000
0204		010

The above circuit configuration shows a 16-bit shift register from SR000 to SR017. The data 000 for address 0203 indicates SR bits 000 ~ 007 and the data 010 for address 0204 indicates SR bits 010 ~ 017. Accordingly, any shift register configuration is possible by changing each data.

■ INTERLOCK (IL)/INTERLOCK CLEAR (ILC) INSTRUCTIONS

The IL and ILC instructions are used in pairs when branching a circuit to plural OUT instructions.



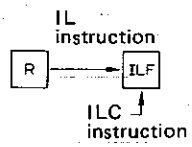
Coding

Address	OP	Data	
0200	LD	0000	
0201	AND	0001	
0202	IL		
0203	LD	0002	*
0204	AND-NOT	0003	
0205	OUT	0050	
0206	LD	0004	
0207	OUT	0051	
0208	ILC		
0209	LD	0005	*

NOTE: * When IL and ILC instructions are used in programming, be sure that an LD instruction will always follow the IL and ILC instructions respectively.

- **Operation of register**

The IL instruction causes the content of the R register to be transferred to the interlock flip-flop (ILF). Accordingly, the ILF is set to "0" if the content of the R register is "0" and to "1" if the content of the R register is "1."

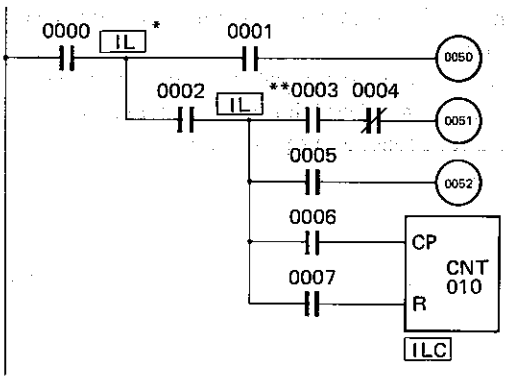


The ILC instruction causes the ILF to be set to "1" irrespective of the content of the R register. In other words, when the IL condition is OFF (i.e., when input 0000 or 0001 is OFF), the state of each relay between the IL and ILC instructions is as follows.

Output relay, internal auxiliary relay	OFF
Timer	Reset
Counter, shift register, latching relay	Holds present state

However, when the IL condition is ON, the state of each relay is the same as that in an ordinary relay circuit without IL/ILC instructions.

- **IL-ILC error**



If IL and ILC instructions are not used in pairs (as in the above example), it is judged as an IL-ILC error during the program check. The operation of the circuit, in this case, will be as programmed, which is shown below.

① If the condition of [IL] * is OFF, output relays 0050, 0051 and 0052 are all OFF and counter CNT10 retains its present count value.

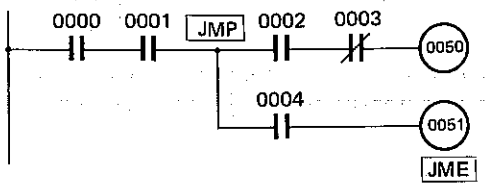
② If the conditions of both [IL] * and [IL] ** are OFF, the state of each relay is the same as ①.

③ If the condition of [IL] * is ON and that of [IL] ** is OFF, output relay 0050 turns ON or OFF if input 0001 is ON or OFF and relays 0051 and 0052 are OFF. Counter CNT010 retains its present count value.

④ If the condition of [IL] * is OFF and that of [IL] ** is ON, the state of each relay is the same as ① and ②.

■ JUMP (JMP)/JUMP END (JME) INSTRUCTIONS

The JMP instruction is used in conjunction with the JME instruction and causes the contents of a program between this instruction and the JME instruction to be ignored or executed according to the result immediately before this instruction.



Coding

Address	OP	Data
0200	LD	0000
0201	AND	0001
0202	JMP	
0203	LD	0002
0204	AND-NOT	0003
0205	OUT	0050
0206	LD	0004
0207	OUT	0051
0206	JME	

- **Operation of register**

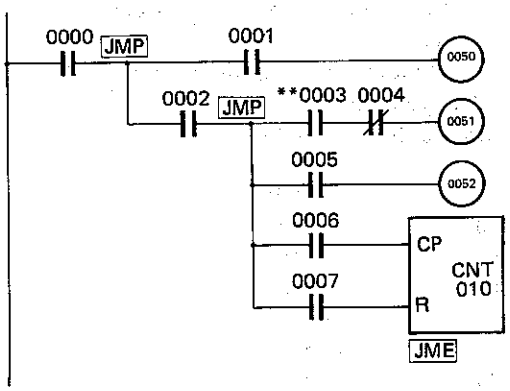
If the content of the R register is "0," the program steps between the JMP and JME instructions are not executed. If the content of the R register is "1," the program steps between the two instructions are executed.

In other words, when the JMP condition is OFF (i.e., when input 0000 or 0001 is OFF), the state of each relay between the JMP and JME instructions are as follows.

Output relay, internal auxiliary relay	Holds present state
Timer	ditto
Counter, shift register	ditto

However, if the JMP condition is ON, the state of each relay is the same as that in an ordinary relay circuit without JMP/JME instructions.

- **JMP-JME error**



If JMP and JME instructions are not used in pairs (as in the above example), it is judged as an JMP-JME error during the program check. The operation of the circuit, in this case, will be as programmed, which is shown below.

① If the condition of [JMP] * is OFF, output relays 0050, 0051 and 0052 remain in their present ON/OFF state, and counter CNT010 retains its present count value.

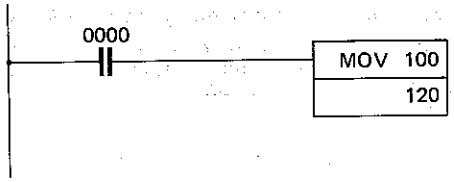
② If the conditions of both [JMP] * and [JMP] ** are OFF, the state of each output relay is the same as ①.

③ If the condition of [JMP] * is ON and that of [JMP] ** is OFF, output relay 0050 turns ON or OFF if input 0001 is ON or OFF, and output relays 0051 and 0052 remain in their present ON/OFF state. Counter CNT010 retains its present count value.

④ If the condition of [JMP] * is OFF and that of [JMP] ** is ON, the state of each output relay is the same as ① and ②.

■ MOVE (MOV)/MOVE NOT (MOV NOT) INSTRUCTIONS

The MOVE instruction is used to transfer the present value of a timer or counter in units of 12 bits and all other data in units of 8 bits. With this instruction, 2-digit constants (00 ~ 99) can also be transferred in units of 8 bits. The MOVE NOT instruction is used to transfer inverted data.



Coding

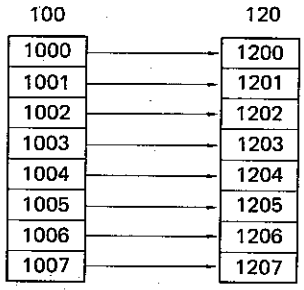
Address	OP	Data
0200	LD	0000
0201	MOV	100
0202		120
0203		

- **Operation of each register**

When the content of the R register is logical 0, nothing will be executed.

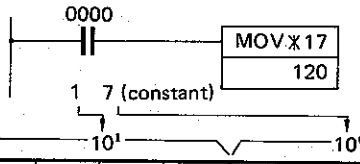
When the content of the R register is logical 1, data will be transferred as follows.

1. Data transfer in units of 8 bits,



According to the program shown above, the data of relay Nos. 1000 ~ 1007 are transferred to the relay Nos. 1200 ~ 1207, respectively.

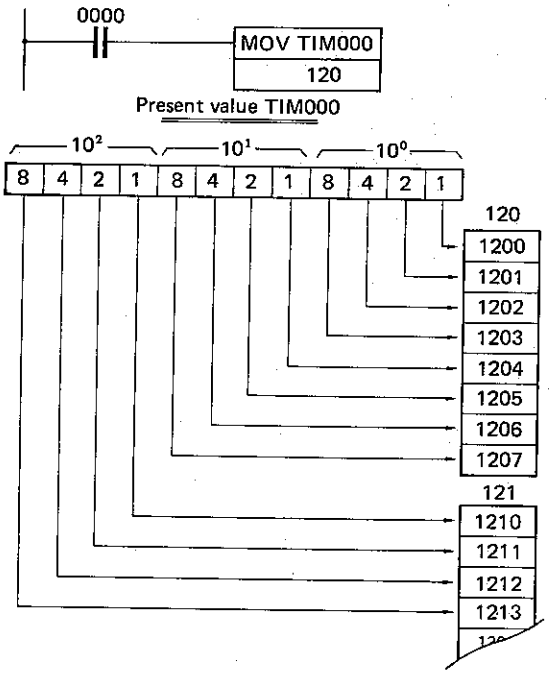
2. To transfer constant,



BCD code	8	4	2	1	8	4	2	1
Relay No.	1207	1206	1205	1204	1203	1202	1201	1200
Data	"0"	"0"	"0"	"1"	"0"	"1"	"1"	"1"

The constant "17" is output to relay Nos. 1200 ~ 1207.

3. To transfer the present value of a timer or counter in units of 12 bits,



The 12-bit data are transferred and relay Nos. 1210 ~ 1213 are automatically assigned to receive the data.

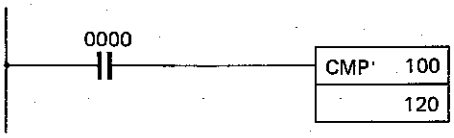
- **MOVE assignment area**

Instruction	1st word: Data (Specifies the data or the relay Nos. or the constant to be transferred)		2nd word: Data (Specifies the relay Nos. by which transferred data are to be received)	
MOV	000 ~ 137	Specifies the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337, or special auxiliary relay Nos. 1340 ~ 1377 in units of 8 bits.*	000 ~ 133	Specifies the data of I/O relay Nos. 0000 ~ 0777 or internal auxiliary relay Nos. 1000 ~ 1337 in units of 8 bits.*
	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**
	SR00 ~ 37	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.**	SR00 ~ 37	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.**
	※00 ~ ※99	Specifies 2-digit constant 00 ~ 99.		
	Timer/ counter Nos. 000 ~ 177	Specifies timer or counter Nos. 000 ~ 177, the present value of which is to be transferred.	000 ~ 132	Specifies the data of I/O relay Nos. 0000 ~ 0777 or auxiliary relay Nos. 1000 ~ 1337 in units of 12 bits.***
			KR00 ~ 36	Specifies the data of latching relay Nos. 000 ~ 377 in units of 12 bits.
			SR00 ~ 36	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.

NOTES:
1. * When the 1st word is entered as "000", the 8 bits of I/O relay Nos. 0000 ~ 0007 are assigned.
2. ** When the 1st word is entered as "KR00", the 8 bits of latching relay Nos. 000 ~ 007 are assigned. In case of SR□□, the shift register assignment is the same as the latching relay Nos.
3. *** When the 1st word is entered as "0020", the 12 bits of I/O relay Nos. 0020 ~ 0033 are assigned.
4. Combination of the 1st and 2nd word data is free.

■ COMPARE (CMP) INSTRUCTION

The COMPARE instruction is used to compare any two 8-bit data to compare an 8-bit data with a 2-digit constant.



Coding

Address	OP	Data
0200	LD	0000
0201	CMP	100
0202		120
0203		

- **Operation of each register**

When the content of the R register is logical 0, the operation result area of special auxiliary relay Nos. 1361 ~ 1363 holds the previous state.

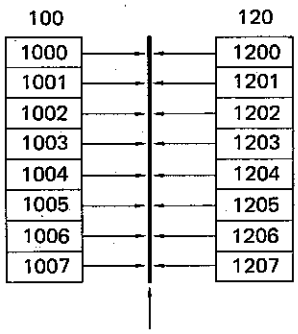
When the content of the R register is logical 1, the 8-bit contents of relay Nos. 1000 ~ 1007 are compared with those of relay Nos. 1200 ~ 1207 and the result of the comparison is output to special auxiliary relay No. 1361, 1362 or 1363.

Special auxiliary relay No. 1361:
The data specified by the 1st word is less than (<) the data specified by the 2nd word.

Special auxiliary relay No. 1362:
The data specified by the 1st word is equal to (=) the data specified by the 2nd word.

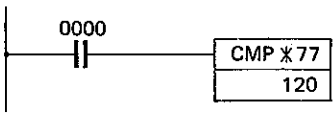
Special auxiliary relay No. 1363:
The data specified by the 1st word is greater than (>) the data specified by the 2nd word.

1. To compare any two 8-bit data,



The results of the comparison are output as follows.
100 < 120 → Special auxiliary relay No. 1361.
100 = 120 → Special auxiliary relay No. 1362.
100 > 120 → Special auxiliary relay No. 1363.

2. To compare 8-bit data with 2-digit constant,



If *77 is specified as the 1st word, the contents of relay Nos. 1200 ~ 1207 are compared with 2-digit BCD constant "77".

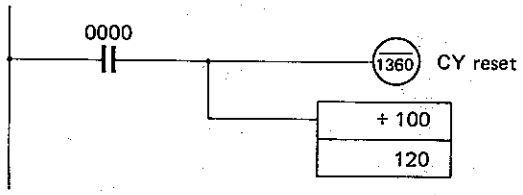
- **COMPARE operation assignment area**

Instruction	1st word: Data (Specifies the data of the relay Nos. or the constant to be compared with the 2nd word data)		2nd word: Data (Specifies the data of the relay Nos. to be compared with the 1st word data)	
CMP	000 ~ 135	Specified the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337 or special auxiliary relay Nos. 1340 ~ 1357 in units of 8 bits.*	000 ~ 135	Specifies the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337, or special auxiliary relay Nos. 1340 ~ 1357 in units of 8 bits.*
	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**
	SR00 ~ 37	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.**	SR00 ~ 37	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.**
	*00 ~ *99	Specifies 2-digit constant 00 ~ 99.		

NOTES:
1. * When the 1st word is entered as "000", the 8 bits of I/O relay Nos. 0000 ~ 0007 are assigned.
2. ** When the 1st word is entered as "KR00", the 8 bits of latching relay Nos. 000 ~ 007 are assigned. In case of SR□□, the shift register assignment is the same as the latching relay Nos.
3. *** When the 1st word is entered as "0020", the 12 bits of I/O relay Nos. 0020 ~ 0033 are assigned.
4. Combination of the 1st and 2nd word data is free.

■ ADD (+) INSTRUCTION

The ADD instruction is used to execute the addition of 2-digit BCD data.



Coding

Address	OP	Data
0200	LD	0000
0201	OUT-NOT	1360
0202	+	100
0203		120

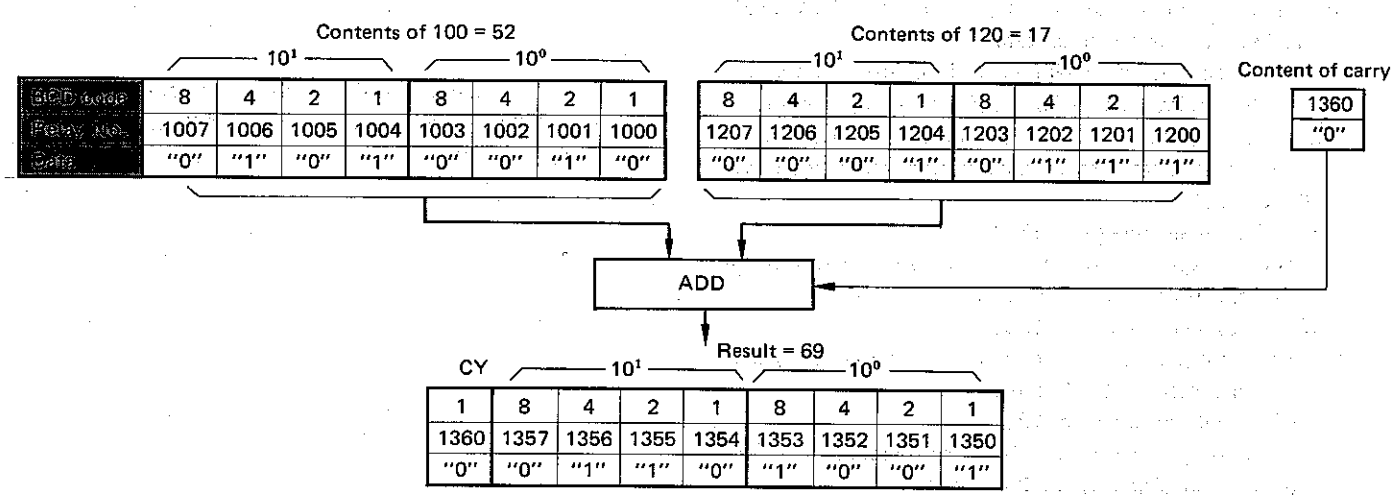
- **Operation of each register**

When the content of the R register is logical 0, only the content of the CY (carry) register (Relay No. 1360) becomes "1" and no addition is executed.

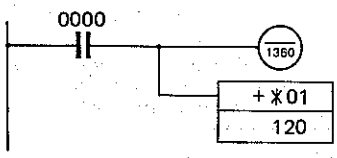
When the content of the R register is logical 1, the 8-bit data of relay Nos. 1000 ~ 1007 are added to the 8-bit data of relay Nos. 1200 ~ 1207, and the result of the addition is output to special auxiliary relay Nos. 1350 ~ 1357 and the content of the CY register to special auxiliary relay No. 1360.

The result of the operation is initialized whenever the mode selector switch of the SYSMAC-M1R is set to the RUN mode. The content of the CY register (1360) is cleared when the END instruction is executed.

1. To add 8-bit data,



2. To add constant,



If ※01 is specified, 2-digit BCD constant "01" is added to the contents of internal auxiliary relay Nos. 1200 ~ 1207.

- Since the CPU doesn't judge whether the data subject to the operation is BCD or not, the result of the operation is indefinite if the BCD value is more than "A" (decimal 10).

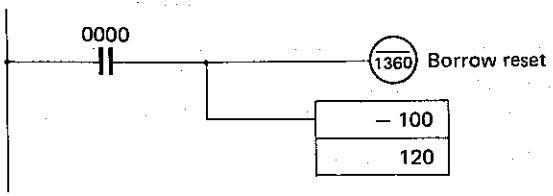
- **ADD operation assignment area**

Instruction	1st word		2nd word	
	Data (Specifies the data of relay Nos. or the constant to be added by the 2nd word data)		Data (Specifies the data of the relay Nos. to be added to the 1st word data)	
ADD (+)	000 ~ 134	Specifies the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337, or special auxiliary relay Nos. 1340 ~ 1347 in units of 8 bits.*	000 ~ 134	Specifies the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337, or special auxiliary relay Nos. 1340 ~ 1347 in units of 8 bits.*
	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**
	SR00 ~ 37	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.**	SR00 ~ 37	Specifies the data of the shift register Nos. 000 ~ 377 in units of 8 bits.**
	✳00 ~ ✳99	Specifies 2-digit constant 00 ~ 99.		

NOTES:
1. * When the 1st word is entered as "000", the 8 bits of I/O relay Nos. 0000 ~ 0007 are assigned.
2. ** When the 1st word is entered as "KR00", the 8 bits of latching relay Nos. 000 ~ 007 are assigned. In case of SR□□, the shift register assignment is the same as the latching relay Nos.
3. *** When the 1st word is entered as "0020", the 12 bits of I/O relay Nos. 0020 ~ 0033 are assigned.
4. Combination of the 1st and 2nd word data is free.

■ SUB (–) INSTRUCTION

The subtract (SUB) instruction is used to execute the subtraction of 2-digit BCD data.



Coding

Address	OP	Data
0200	LD	0000
0201	OUT·NOT	1360
0202	–	100
0203		120

- **Operation of each register**

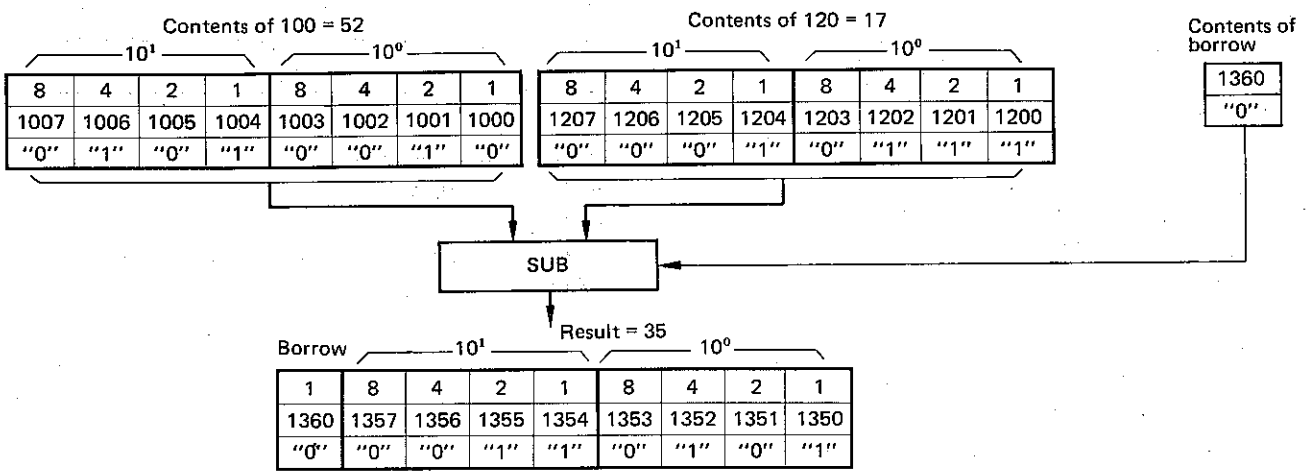
When the content of the R register is logical 0, only the content of the Borrow register (1360) becomes "1" and no subtraction is not executed.

When the content of the R register is logical 1, the 8-bit data of relay Nos. 1200 ~ 1207 are subtracted from the 8-bit data of relay Nos. 1000 ~ 1007 and the result of the subtraction is output to special auxiliary relay Nos. 1350 ~ 1357 and the content of the Borrow register to special auxiliary relay No. 1360.

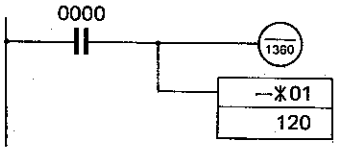
The result of the operation is initialized whenever the mode selector switch of the SYSMAC-M1R is set to the RUN mode.

The content of the Borrow register (1360) is cleared when the END instruction is executed.

1. To subtract 8-bit data,



2. To subtract constant,



If *01 is specified, 2-digit BCD constant "01" is subtracted from the contents of internal auxiliary relay Nos. 1200 ~ 1207.

- Since the CPU doesn't judge whether the data subject to the operation is BCD or not, the result of the operation is indefinite if the BCD value is more than "A (decimal 10)."

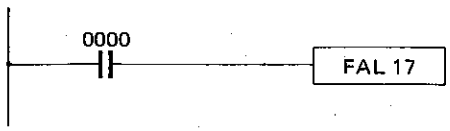
- **SUB operation assignment area**

Instruction	1st word: Data (Specifies the data of relay Nos. or the constant to be subtracted by the 2nd word data)		2nd word: Data (Specifies the data of the relay Nos. to be subtracted from the 1st word data)	
SUB (–)	000 ~ 134	Specifies the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337, or special auxiliary relay Nos. 1340 ~ 1347 in units of 8 bits.*	000 ~ 134	Specifies the data of I/O relay Nos. 0000 ~ 0777, internal auxiliary relay Nos. 1000 ~ 1337, or special auxiliary relay Nos. 1340 ~ 1347 in units of 8 bits.*
	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**	KR00 ~ 37	Specifies the data of latching relay Nos. 000 ~ 377 in units of 8 bits.**
	SR00 ~ 37	Specifies the data of shift register Nos. 000 ~ 377 in units of 8 bits.**	SR00 ~ 37	Specifies the data of the shift register Nos. 000 ~ 377 in units of 8 bits.**
	*00 ~ *99	Specifies 2-digit constant 00 ~ 99.		

NOTES:
1. * When the 1st word is entered as "000", the 8 bits of I/O relay Nos. 0000 ~ 0007 are assigned.
2. ** When the 1st word is entered as "KR00", the 8 bits of latching relay Nos. 000 ~ 007 are assigned. In case of SR□□, the shift register assignment is the same as the latching relay Nos.
3. ** When the 1st word is entered as "0020", the 12 bits of I/O relay Nos. 0020 ~ 0033 are assigned.
4. Combination of the 1st and 2nd word data is free.

■ DIAGNOSTIC (FAL) INSTRUCTION

The FAL instruction is used to output the failure or abnormal mode to the FAL area indicating the occurrence of a failure or abnormality in the internal circuit during the operation of the SYSMAC-M1R. To use this instruction, circuits which are presumed to fail or become abnormal must be programmed beforehand with a failure or abnormal mode (01 ~ 99) assigned to each of the faulty or abnormal circuits.



Coding

Address	OP	Data
0200	LD	0000
0201	FAL	17
0202		
0203		

- **Operation of each resister**
  When the content of the R register is logical 0, nothing is executed.

- When the content of the R register is logical 1, the failure or abnormal mode (01 ~ 99) is output in 2-digit BCD to special auxiliary relay Nos. 1340 ~ 1347. The value once stored in the FAL area is not cleared until execution of the FAL00 instruction. When the FAL00 instruction is executed, the next value is acceptable by the FAL area.

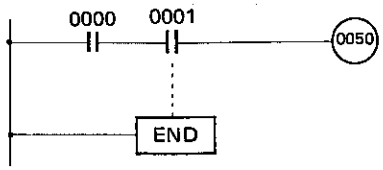
FAL area (17)

	10^1				10^0			
BCD code	8	4	2	1	8	4	2	1
Relay No.	1347	1346	1345	1344	1343	1342	1341	1340
Data	"0"	"0"	"0"	"1"	"0"	"1"	"1"	"1"

- **Values that can be assigned**
  FAL00 .... Clear
  FAL01 ~ FAL99 } Failure or abnormal mode 01 ~ 99

■ END INSTRUCTION

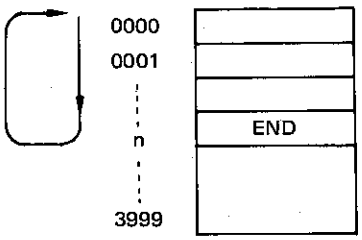
Insert this instruction at the end of a program.



Coding

Address	OP	Data
0000	LD	0001
0001	AND	0002
0002	OUT	0050
0003	⋮	⋮
0004	⋮	⋮
⋮	⋮	⋮
n	END	—

- The program memory of the SYSMAC-M1R is provided with addresses 0000 to 3999. The CPU scans program data from address 0000 to the address with an END instruction according to the sequence diagram.



- When performing a test run, insert an END instruction at each end of a sequence circuit and then delete the END instruction after confirming each circuit. In this manner, the test run can be executed smoothly.

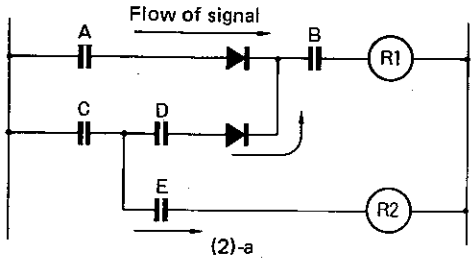
5. Programming

5.1 How to Program

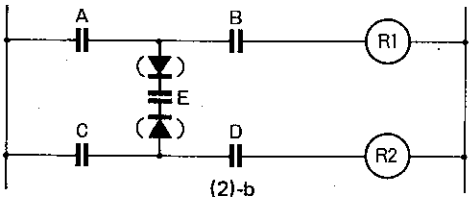
With the SYSMAC-M1R, a sequence circuit controlled according to the sequence of the instructions stored in the CPU memory. Therefore, it is necessary to observe the hints on correct programming and programming order.

■ HINTS ON CORRECT PROGRAMMING

1. Since the number of contacts is not limited for input/output relays, internal auxiliary relays, timers, etc., it can be said that the best way to design a sequence circuit is to configure a simple, clear circuit, rather than a complicated circuit created by reducing the number of contacts.
2. In the SYSMAC-M1R, signals will flow from the left to the right. In other words, signals will flow as if diodes are inserted in the circuit as shown in (2)-a or (2)-b. To operate a circuit without diodes in the same manner as the circuit configured with general control relays, it is necessary to rewrite the circuit.

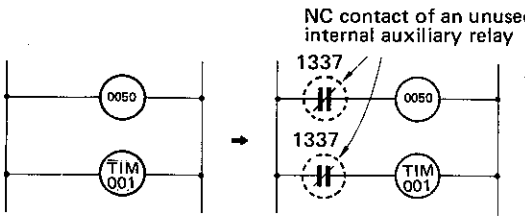


(2)-a

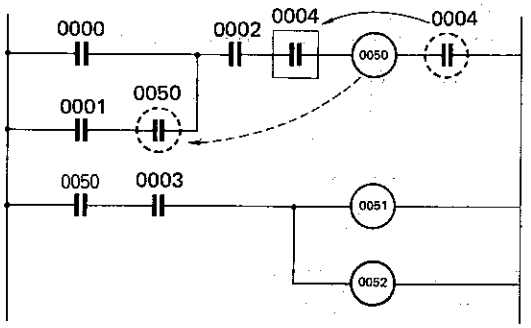


(2)-b

3. In a series-parallel circuit, the number of contacts that can be connected in series is not limited, as well as the number of contacts that can be connected in parallel.
4. No output relay can be connected directly from the bus bar. If necessary, connect it through the NC contact of an unused internal auxiliary relay or special auxiliary relay 1365.



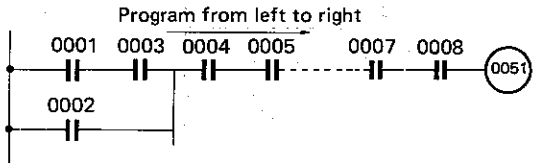
5. All output relays are provided with auxiliary contacts that can be used on a circuit, in addition to the output signal contacts to drive loads actually. The number of contacts that can be used per output relay is not limited.



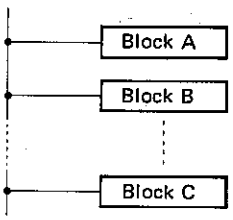
6. No relay contact can be inserted next to an output coil. If necessary, insert it before the output coil.
7. Two or more output coils can be connected in parallel.
8. For contact and coil numbers on the circuit, use the I/O relay numbers described in Section 3.1.
9. Output coil numbers (including those for timers, counters, shift registers and latching relays) cannot be used in duplication.

■ PROGRAMMING ORDER

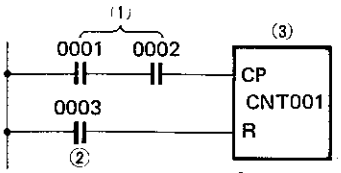
1. Program a circuit from its left to right.



2. Assume the circuit elements located from the bus bar to an output relay as one block. If a number of blocks are in line, programming can be started from any block. However, pay attention in case of circuits utilizing scan time or timing such as differentiator, shift register, etc.



3. When composite instructions such as timer, counter, shift register, latching relay, etc. are used, their order of programming is predetermined. Be sure to perform the programming according to the predetermined order.

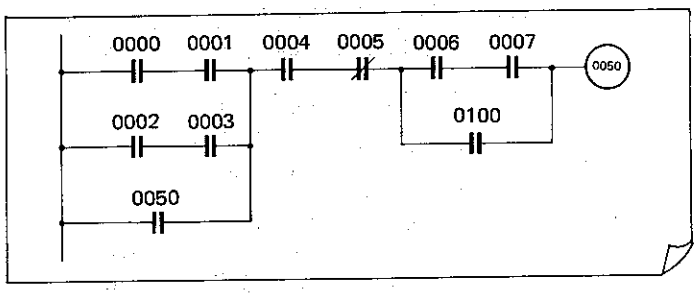


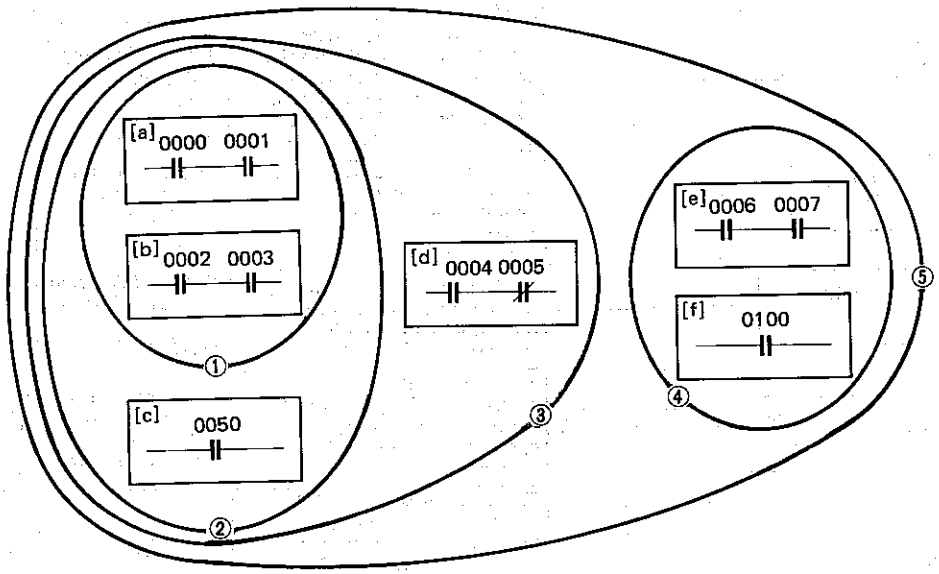
Program in the order of ① → ③.

Address	OP	Data
⋮		⋮
n	LD	0001
n + 1	AND	0002
n + 2	LD	0003
n + 3	CNT	001
n + 4		056
⋮		⋮

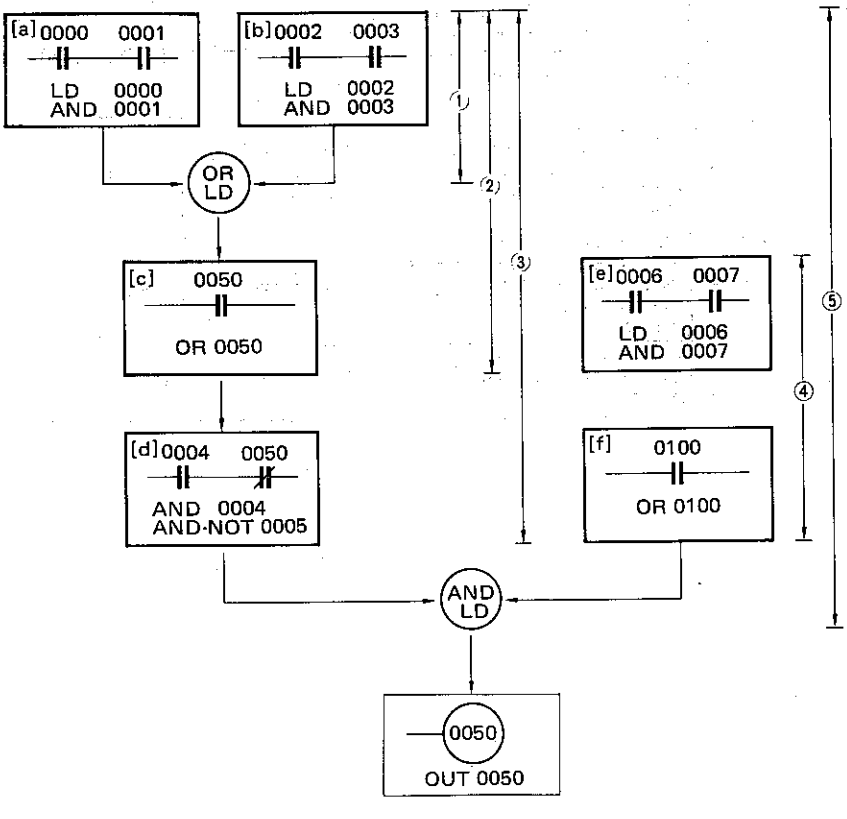
4. Be sure to insert an END instruction at the end of each program.
5. A ladder diagram such as the one shown below can be divided into small blocks as shown below, to program each block in the order of ① to ⑤. Eventually, the circuit will be programmed as one large block such as ⑤.

- **Ladder diagram**





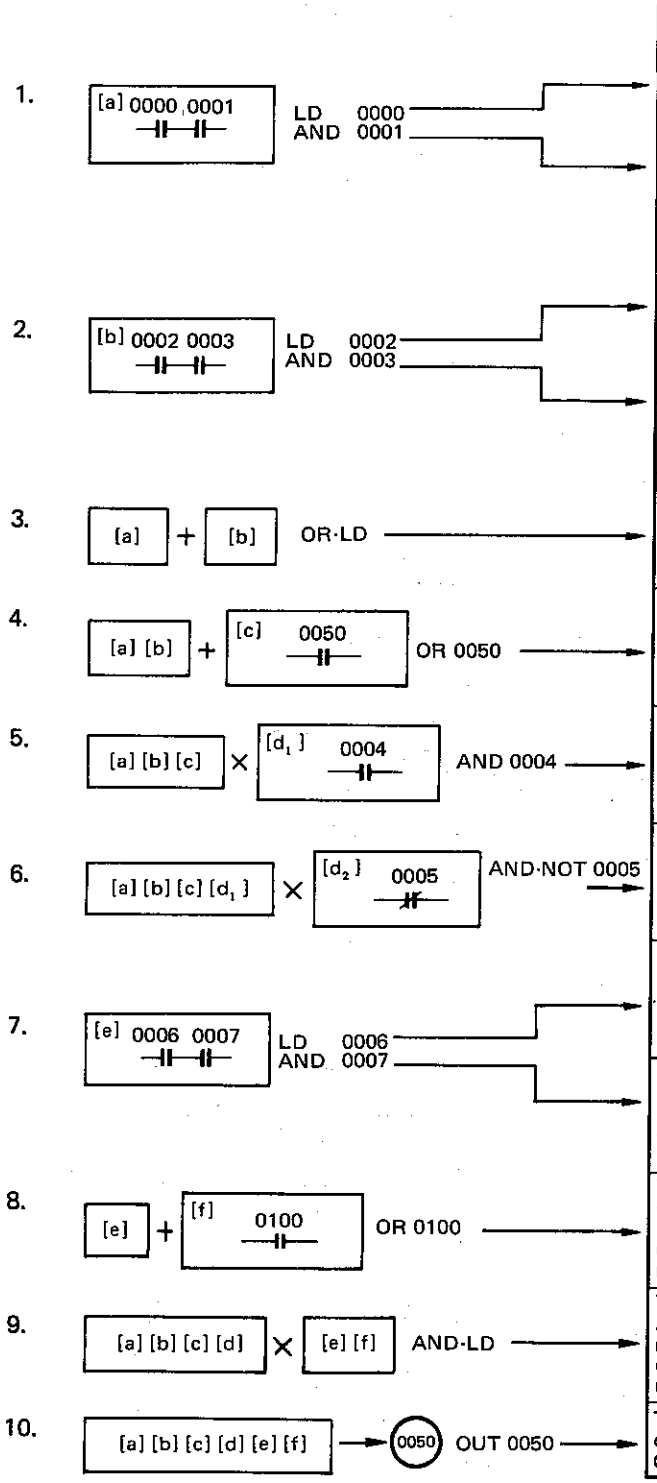
- **Programming procedure**



- **Coding**

Address	OP	Data
0000	LD	0000
0001	AND	0001
0002	LD	0002
0003	AND	0003
0004	OR·LD	
0005	OR	0050
0006	AND	0004
0007	AND-NOT	0005
0008	LD	0006
0009	AND	0007
0010	OR	0100
0011	AND-LD	
0012	OUT	0050
⋮		⋮
n	END	

- **Operations of R and S registers**

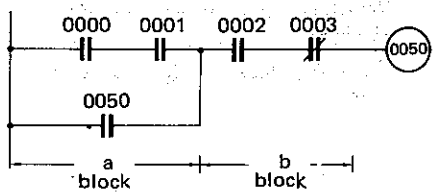


Content of register	R register	S register
The content ("1" or "0") of 0000 is stored in R register.	0000	Vacant
The content of R register is ANDed with the content of 0001 and the result of operation is stored in R register.	Result of 0000 0001 = [a]	Vacant
The previous content of R register is transferred to S register and the content of 0002 is newly stored in R register.	0002	[a]
The content of R register is ANDed with the content of 0003, and the result of operation is stored in R register.	Result of 0002 0003 = [b]	[a]
The content of R register (result [b]) is ORed with the content of S register (result [a]), and the result of operation is stored in R register.	Result of ORing [a] with [b] = [a] [b]	Vacant
The content of 0050 is ORed with the content of R register, and the result of operation is stored in R register.	Result of ORing [a] [b] with [c] = [a] [b] [c]	Vacant
The content of 0004 is ANDed with the content of R register, and the result of operation is stored in R register.	Result of ANDing [a] [b] [c] with [d_1] = [a] [b] [c] [d_1]	Vacant
The content of 0005 is ANDed with the content of R register and the result of operation is stored in R register.	Result of ANDing [a] [b] [c] [d_1] with [d_2] = [a] [b] [c] [d]	Vacant
The previous content of R register is transferred to S register, and the content of 0006 is stored in R register.	0006	[a] [b] [c] [d]
The content of R register is ANDed with the content of 0007, and the result of operation is stored in R register.	Result of 0006 0007 = [e]	[a] [b] [c] [d]
The content of R register is ORed with the content of 0100, and the result of operation is stored in R register.	Result of ORing [e] with [f] = [e] [f]	[a] [b] [c] [d]
The content of R register is ANDed with the content of S register, and the result of operation is stored in R register.	[a] [b] [c] [d] [e] [f]	Vacant
The result of R register is output to output relay OUT0050.	[a] [b] [c] [d] [e] [f]	Vacant

5.2 Applied Programs

■ WHEN LD/OR/AND/NOT INSTRUCTIONS ARE USED

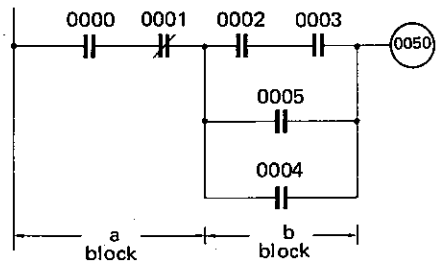
1. An example of parallel-series circuit



OP	Data	
LD	0000	a
AND	0001	
OR	0050	
AND	0002	b
AND-NOT	0003	
OUT	0050	
⋮	⋮	
END		

- Process block b after programming block a (parallel circuit).
- For coding, enter I/O relay numbers in the data field.

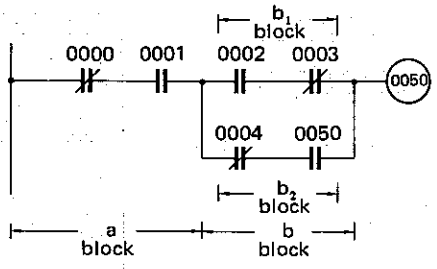
2. An example of series-parallel circuit



OP	Data	
LD	0000	a
AND-NOT	0001	
LD	0002	b
AND	0003	
OR	0050	
OR	0004	
AND-LD		
OUT	0050	
⋮	⋮	
END		

- Divide the circuit into blocks a and b and program each block.
- Then combine blocks a and b by AND-LD instruction.

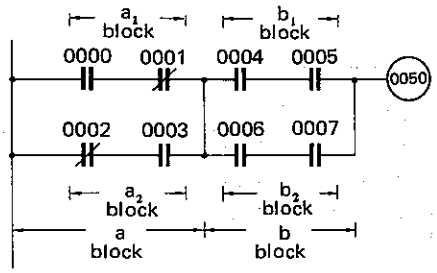
3. An example of series-parallel circuit



OP	Data	
LD-NOT	0000	a
AND	0001	
LD	0002	b_1
AND-NOT	0003	
LD-NOT	0004	b_2
AND	0050	
OR-LD		b_1+b_2
AND-LD		a·b
OUT	0050	
⋮	⋮	
END		

- Program block a.
- Program block b_1 and then block b_2.
- Combine blocks b_1 and b_2 using OR-LD instruction.
- Combine blocks a and b using AND-LD instruction.

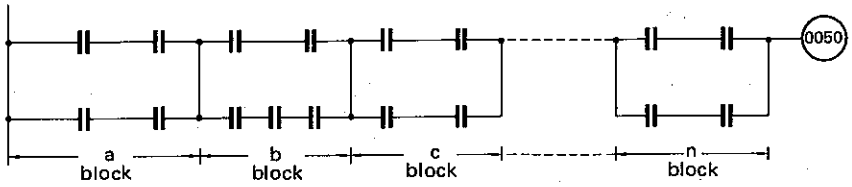
4. An example of connecting parallel circuits in series.



OP	Data	
LD	0000	a_1
AND-NOT	0001	
LD-NOT	0002	a_2
AND	0003	
OR-LD		a_1+a_2
LD	0004	b_1
AND	0005	
LD	0006	b_2
AND	0007	
OR-LD		b_1+b_2
AND-LD		a·b
OUT	0050	
⋮	⋮	
END		

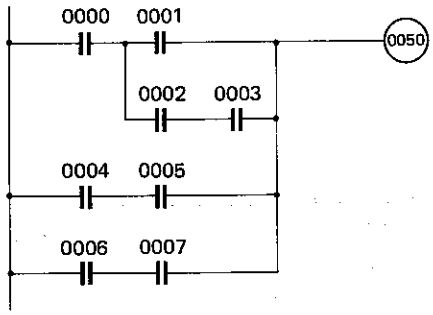
- Program block a_1 and then block a_2 and combine both blocks using OR-LD instruction.
- Program blocks b_1 and b_2 in the same manner as above.
- Combine blocks a and b using AND-LD instruction.

5. An example of connecting parallel circuits in series



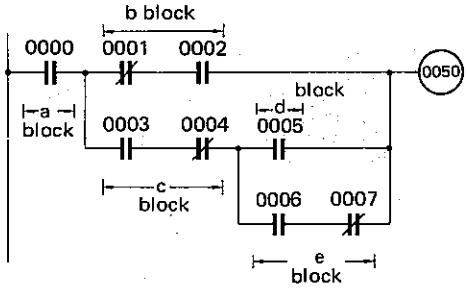
- When a number of blocks continue from block number a to n, the programming procedure is the same as paragraph 4 above. Namely, program the circuit in the following sequence.
  ① block a → ② block b → ③ blocks a·b → ④ block c → ⑤ blocks a·b·c → ⑥ .....

6. An example of complicated parallel circuit



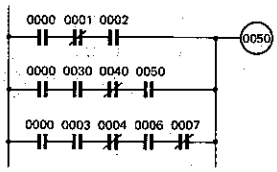
OP	Data
LD	0000
LD	0001
LD	0002
AND	0003
OR·LD	
AND·LD	
LD	0004
AND	0005
OR·LD	
LD	0006
AND	0007
OR·LD	
OUT	0050
⋮	⋮
END	

7. An example of complicated circuit



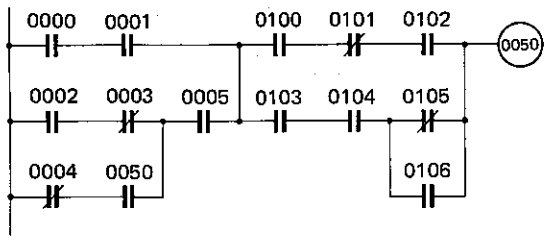
OP	Data	
LD	0000	a
LD·NOT	0001	b
AND	0002	
LD	0003	c
AND·NOT	0004	
LD	0005	d
LD	0006	e
AND·NOT	0007	
OR·LD		d+e
AND·LD		(d+e)·c
OR·LD		(d+e)·c+b
AND·LD		[(d+e)·c+b]·a
OUT	0050	
⋮	⋮	
END		

- The circuit shown on the left may be re-written as follows.



OP	Data
LD	0000
AND·NOT	0001
AND	0002
LD	0000
AND	0003
AND·NOT	0004
AND	0005
OR·LD	
LD	0000
AND	0003
AND·NOT	0004
AND	0006
AND·NOT	0007
OR·LD	
OUT	0050
⋮	⋮
END	

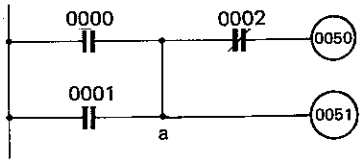
8. An example of complicated circuit



OP	Data
LD	0000
AND	0001
LD	0002
AND·NOT	0003
LD·NOT	0004
AND	0050
OR·LD	
AND	0005
OR·LD	
LD	0100
AND·NOT	0101

OP	Data
AND	0102
LD	0103
AND	0104
LD·NOT	0105
OR	0106
AND·LD	
OR·LD	
AND·LD	
OUT	0050
⋮	⋮
END	

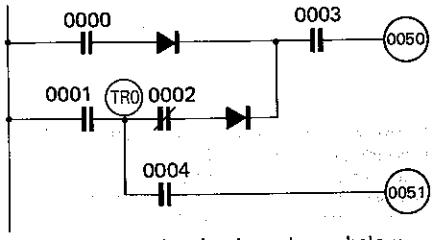
9. An example of circuit requiring caution



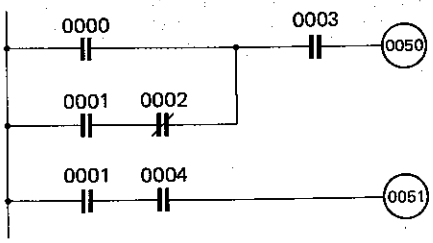
OP	Data
LD	0000
OR	0001
OUT	0051
AND-NOT	0002
OUT	0050
⋮	⋮
END	

- In such a case as shown on the left, program relay contact: $\dashv\!\overset{0002}{/}\!\vdash$ after programming output relay 0051. This action is necessary for the following reason. Even if an output is sent to output relay 0050, the content of the R register at point a will remain unchanged. However, if $\dashv\!\overset{0002}{/}\!\vdash$ is programmed before output relay 0050, the content of the R register at point a will change and differ from the content sent to output relay 0051.

10. An example of circuit requiring caution



Separate the circuit as shown below.

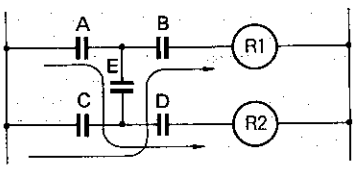


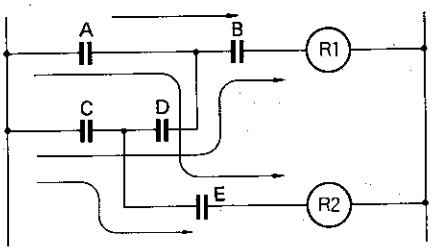
OP	Data
LD	0000
LD	0001
AND-NOT	0002
OR-LD	
AND	0003
OUT	0050
LD	0001
AND	0004
OUT	0051
⋮	⋮
END	

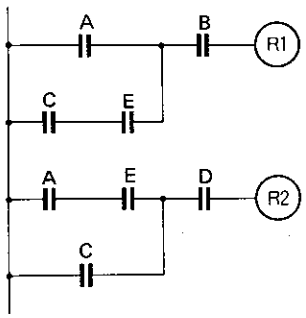
- If the circuit is to be programmed without separating it, program a temporary memory relay after relay contact $\dashv\!\overset{0001}{/}\!\vdash$. The following table shows an example of programming (TR0) after $\dashv\!\overset{0001}{/}\!\vdash$.

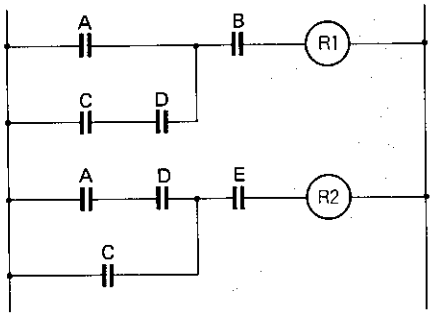
OP	Data
LD	0000
LD	0001
OUT-TR	0
AND-NOT	0002
OR-LD	
AND	0003
OUT	0050
LD-TR	0
AND	0004
OUT	0051
⋮	⋮
END	

11. Examples of circuit requiring rewrite







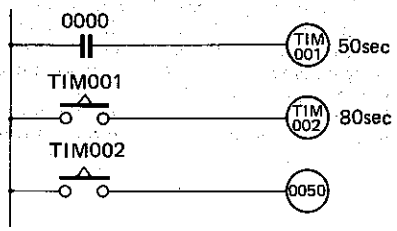


- Such circuits as shown on the upper left cannot be programmed and must therefore be rewritten as shown directly below.
- Since the two upper circuits are respectively configured with control relays, the circuits operate even by the flows of signals shown by the arrows. To permit the similar circuit operation with the SYSMAC-M1R, the two upper circuits must be rewritten into the corresponding circuits shown below.

■ WHEN TIM/CNT INSTRUCTIONS ARE USED

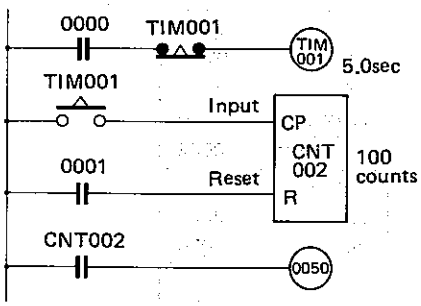
1. Long-time timer

a. Series connection of TIM instructions



OP	Data
LD	0000
TIM	001
	500
LD-TIM	001
TIM	002
	800
LD-TIM	002
OUT	0050
⋮	⋮
END	

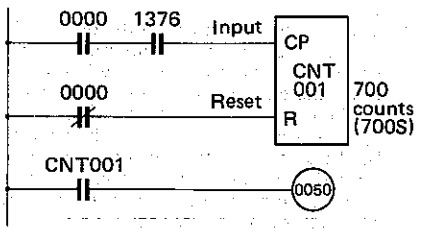
b. Use of CNT instruction (e.g., 500sec)



OP	Data
LD	0000
AND-NOT-TIM	001
TIM	001
	050
LD-TIM	001
LD	0001
CNT	002
	100
LD-CNT	002
OUT	0050
⋮	⋮
END	

- In this circuit, a pulse is generated every 5 seconds by timer TIM001 and then pulses at intervals of 5 seconds are counted by counter CNT002. The example shown here is a 500sec timer. The setting time of the timer is (timer + scan time) x number of counts.
- The present count value of the counter is retained in memory even if the power switch of the SYSMAC-M1R is turned off.

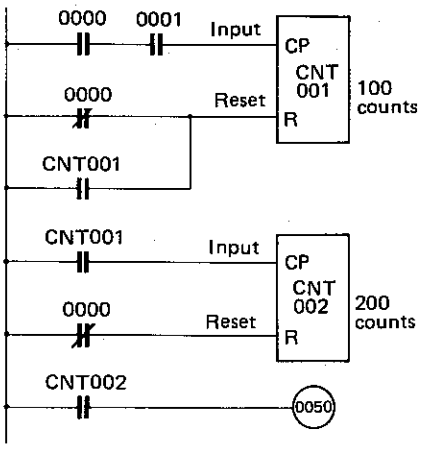
c. Use of internal clock pulse (e.g., 700sec)



OP	Data
LD	0000
AND	1376
LD-NOT	0000
CNT	001
	700
LD-CNT	001
OUT	0050
⋮	⋮
END	

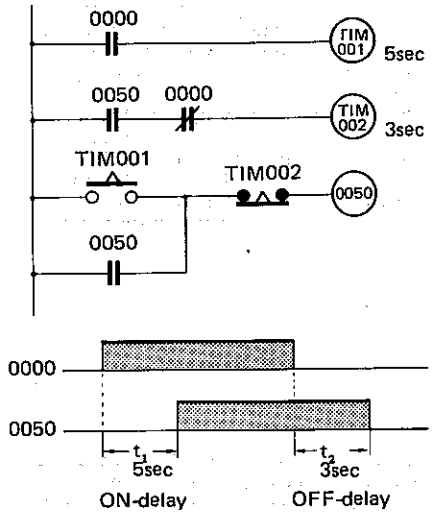
- The SYSMAC-M1R has three types of internal clock pulses (0.2sec clock: 1375, 1sec clock: 1376, 0.1sec clock: 1377). By counting any of type of pulses with a counter, a long-time timer can be developed.
- As CNT instruction is employed, the present count value is retained in memory even after the power is turned off.

2. Multi-digit counter (e.g., 20,000 counts)



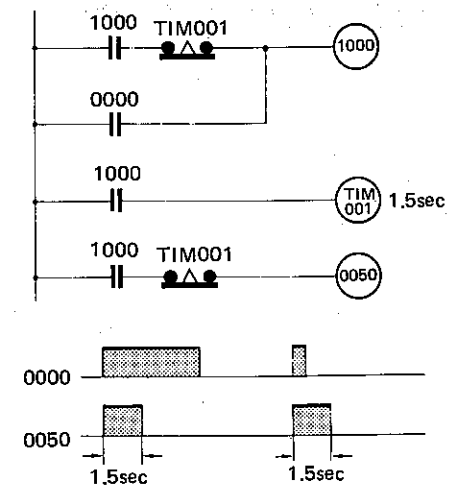
OP	Data
LD	0000
AND	0001
LD-NOT	0000
OR-CNT	001
CNT	001
	100
LD-CNT	001
LD-NOT	0000
CNT	002
	200
LD-CNT	002
OUT	0050
⋮	⋮
END	

3. An example of ON/OFF-delay timer circuit



OP	Data
LD	0000
TIM	001
	050
LD	0050
AND·NOT	0000
TIM	002
	030
LD·TIM	001
OR	0050
AND·NOT·TIM	002
OUT	0050
⋮	⋮
END	

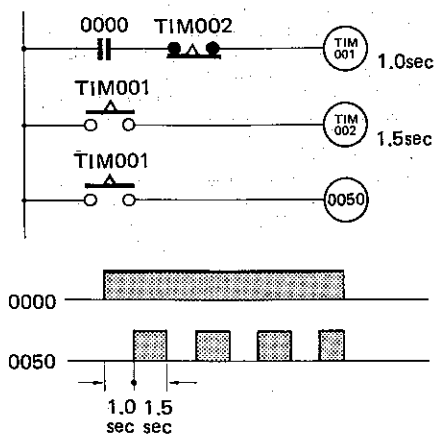
4. An example of one-shot timer circuit



OP	Data
LD	1000
AND·NOT·TIM	001
OR	0000
OUT	1000
LD	1000
TIM	001
	015
LD	1000
AND·NOT·TIM	001
OUT	0050
⋮	⋮
END	

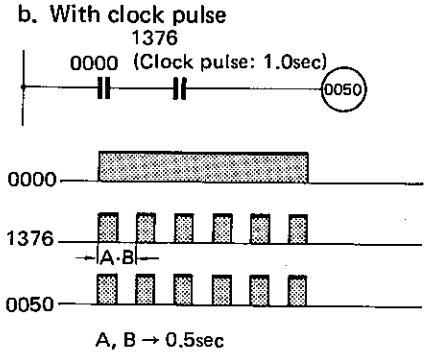
- One shot output is produced for only the set time of TIM001 after an input signal is applied. (Input 0000 > scan time)

5. Examples of flicker circuit
   a. With 2 timers used



OP	Data
LD	0000
AND·NOT·TIM	002
TIM	001
	010
LD·TIM	001
TIM	002
	015
LD·TIM	001
OUT	0050
⋮	⋮
END	

b. With clock pulse

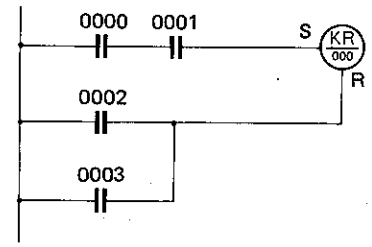


OP	Data
LD	0000
AND	1376
OUT	0050
⋮	⋮
END	

- Using an internal clock pulse (0.1sec, 1.0sec or 0.2sec), a flicker circuit can be processed easily. In this case, however, the flickering time is available only in the following 3 types.
  Special auxiliary relay number 1375: 0.2sec clock pulse
  Special auxiliary relay number 1376: 1.0sec clock pulse
  Special auxiliary relay number 1377: 0.1sec clock pulse

■ WHEN LATCHING RELAY IS USED

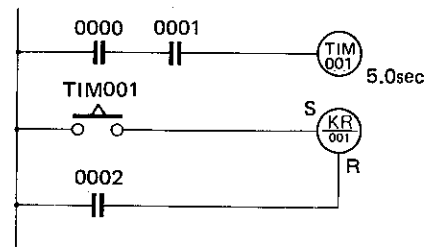
1. Basic circuit



OP	Data
LD	0000
AND	0001
LD	0002
OR	0003
KR	000
⋮	⋮
END	

- In the event of a power failure, the ON/OFF state before the power failure can be retained in memory, using a latching relay. SYSMAC-M1R has 256 latching relays with relay numbers KR000 ~ KR377.
- Memory retention time after a power failure is about 2 years just the same as that of the program memory.

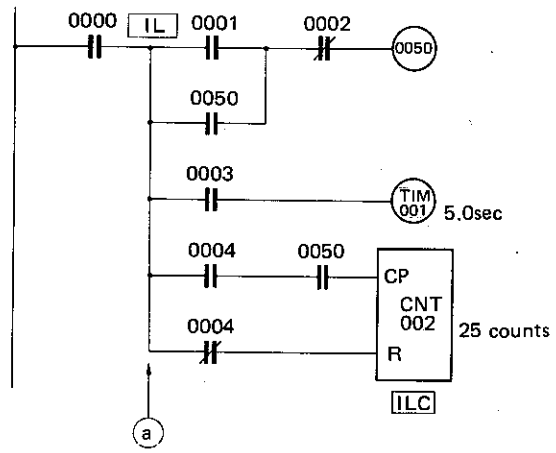
2. A circuit to keep the time-up state



OP	Data
LD	0000
AND	0001
TIM	001
	050
LD·TIM	001
LD	0002
KR	001
⋮	⋮
END	

■ WHEN IL/ILC INSTRUCTIONS ARE USED

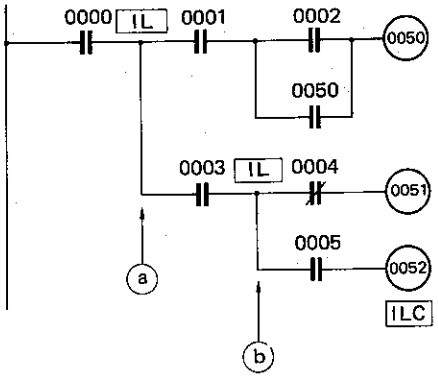
1. Basic circuit



OP	Data
LD	0000
IL	
LD	0001
OR	0050
AND-NOT	0002
OUT	0050
LD	0003
TIM	001
	050
LD	0004
AND	0050
LD-NOT	0004
CNT	002
	025
ILC	
⋮	⋮
END	

- Program the circuit by taking the common line ⓐ after the IL instruction, as a bus bar.
- An ILC instruction must always be added to the end of a circuit employing an IL instruction. The instructions between the IL and ILC instructions are executed.
- When input 0000 is OFF, timer TIM001 is reset but the present value of counter CNT002 is retained.
- When preparing an automatic/manual circuit, the circuit shown on the left can be operated only in the automatic mode by turning input 0000 on automatically.

2. Output branching circuit

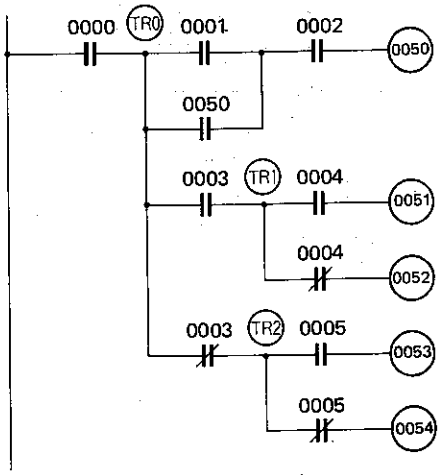


OP	Data
LD	0000
IL	
LD	0001
LD	0002
OR	0050
AND-LD	
OUT	0050
LD	0003
IL	
LD-NOT	0004
OUT	0051
LD	0005
OUT	0052
ILC	
⋮	⋮
END	

- IL instructions can be used for programming an output branching circuit (i.e., tree circuit).
- IL instructions can be used in as many stages as required, though this condition is regarded as an IL/JMP error during the program check.
  Each time an IL instruction is programmed, the bus bar changes from ⓐ to ⓑ.

■ WHEN TR INSTRUCTIONS ARE USED

1. Output branching circuit

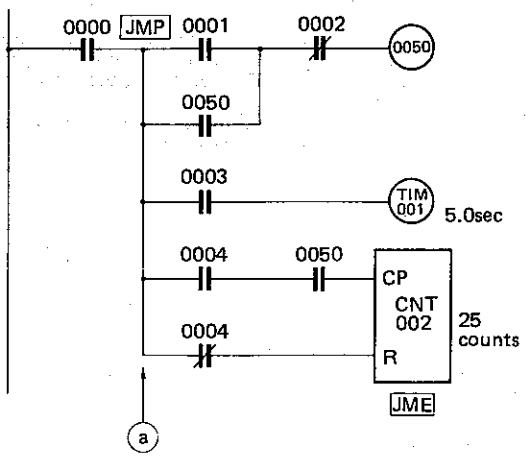


OP	Data
LD	0000
OUT-TR	0
LD-TR	0
LD	0001
OR	0050
AND-LD	
AND	0002
OUT	0050
LD-TR	0
AND	0003
OUT-TR	1
LD-TR	1
AND	0004
OUT	0051
LD-TR	1
AND-NOT	0004
OUT	0052
LD-TR	0
AND-NOT	0003
OUT-TR	2
LD-TR	2
AND	0005
OUT	0053
LD-TR	2
AND-NOT	0005
OUT	0054
⋮	⋮
END	

- In case of an output branching circuit, temporary memory relays (TR0 ~ TR7) are used at each branch point.
- Temporary memory relay coil numbers cannot be used in duplication within the same block. With two or more blocks, they can be used in duplication.

■ WHEN JMP/JME INSTRUCTIONS ARE USED

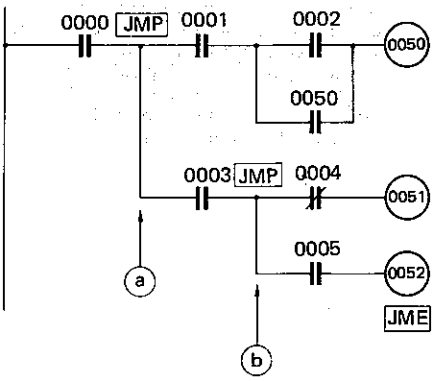
1. Basic circuit



OP	Data
LD	0000
JMP	
LD	0001
OR	0050
AND-NOT	0002
OUT	0050
LD	0003
TIM	001
	050
LD	0004
AND	0050
LD-NOT	0004
CNT	002
	025
JME	
⋮	⋮
END	

- Program the circuit by taking the common line ⓐ after the JMP instruction, as a bus bar.
- A JME instruction must always be added to the end of a circuit employing a JMP instruction.
- When input 0000 is ON, the instructions between the JMP and JME instructions are executed.
- When input 0000 is OFF, output relay 0050, timer TIM0001 and counter CNT002 retain their state immediately before the input is turned off.

2. Output branching circuit

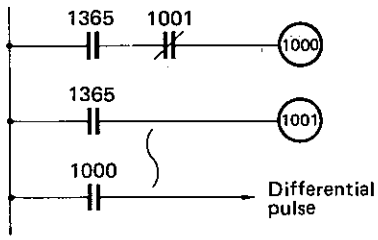


OP	Data
LD	0000
JMP	
LD	0001
LD	0002
OR	0050
AND-LD	
OUT	0050
LD	0003
JMP	
LD-NOT	0004
OUT	0051
LD	0005
OUT	0052
JME	
⋮	⋮
END	

- JMP instructions can be used in as many stages as required, although this condition is regarded as an IL/JMP error during the program check.
- Each time a JME instruction is programmed, the bus bar changes from ⓐ to ⓑ.
- When input 0000 is ON, the instructions between the JMP and JME instructions are executed.
- When input 0000 is OFF, output relays 0050, 0051 and 0052 retain their ON/OFF state immediately before the input is turned off.

■ 1-CYCLE DIFFERENTIATION

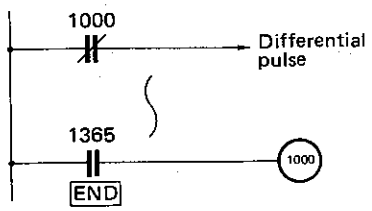
1.



OP	Data
LD	1365
AND-NOT	1001
OUT	1000
LD	1365
OUT	1001
≀	
LD	1000
⋮	⋮
END	

- Special auxiliary relay 1365 is normally ON. Shown here is a 1-cycle differentiation circuit when power is applied, using special auxiliary relay 1365.

2.

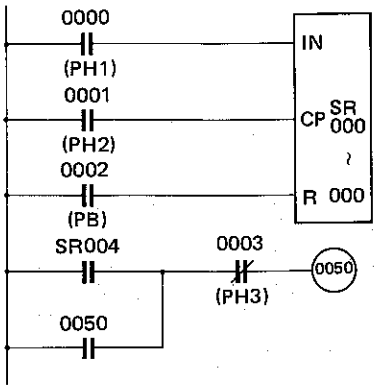


OP	Data
≀	
LD· NOT	1000
≀	
LD	1365
OUT	1000
END	

- Shown here is a 1-cycle differentiation circuit when power is applied, using special auxiliary relay 1365. In this case, be sure to program the instruction "OUT1000" at the end of the program.

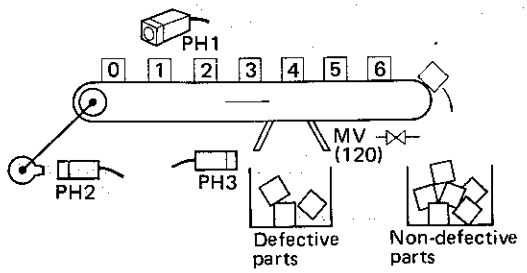
■ WHEN SR INSTRUCTIONS ARE USED

1. Defect detecting circuit (1-stage, 8-bit shift register)

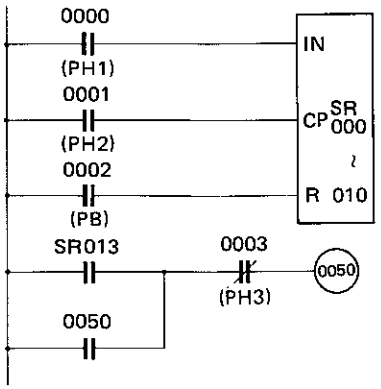


OP	Data
LD	0000
LD	0001
LD	0002
SR	000
	000
LD·SR	004
OR	0050
AND·NOT	0003
OUT	0050
⋮	⋮
END	

- This circuit can be used for such operations in a product inspection line as sorting defective products from non-defective products and distributing them with a cylinder.
- By specifying a shift register as SR000 → 000, shift register bits SR000 to SR007 can be operated to obtain the output of each bit arbitrarily.
- Data in excess of 8 bits are automatically cleared from the first-in data.



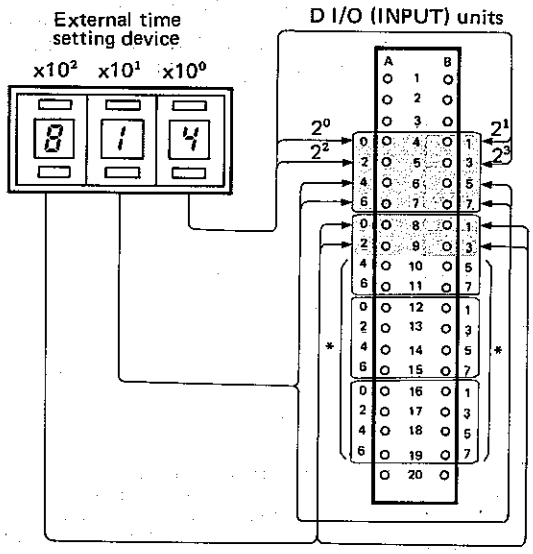
2. Multi-stage shift register (2-stage, 16-bit shift register)



OP	Data
LD	0000
LD	0001
LD	0002
SR	000
	010
LD·SR	013
OR	0050
AND·NOT	0003
OUT	0050
⋮	⋮
END	

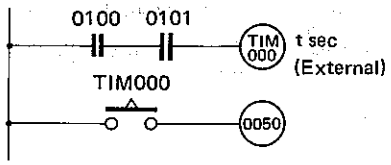
■ WHEN TIMER OR COUNTER IS USED THROUGH EXTERNAL SETTING

1. Timer



NOTE: * This area can be used for other inputs.

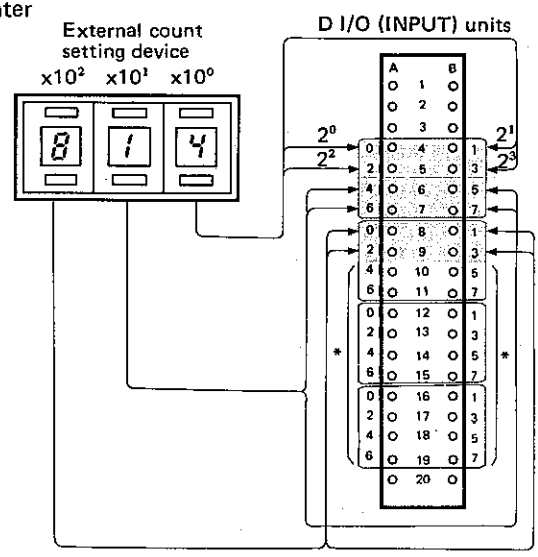
- By connecting an external 3-digit time setting device to input relay Nos. 0000 ~ 0013, the data of the external setting device is used as the setting time of the timer.



OP	Data
LD	0100
AND	0101
TIM	000
✳	00
LD TIM	000
OUT	0050

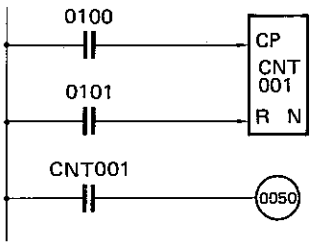
- TIM000 operates for 81.4sec according to the data of the external setting device shown in the above figure.
- When ✳ is entered into the TIM time setting area, external setting is specified.
- For example, when ✳00 is entered, relay Nos. 0000 ~ 0007 and 0010 ~ 0013 are assigned as the external terminals for external setting.
  Also, when ✳02 is entered, relay Nos. 0020 ~ 0027 and 0030 ~ 0033 are assigned as the external terminals.

2. Counter



NOTE: * This area can be used for other inputs.

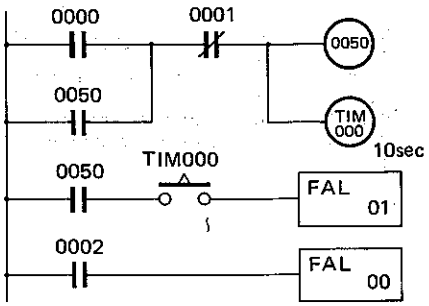
- By connecting an external 3-digit count setting device to input relay Nos. 0000 ~ 0017, the data of the external setting device is used as the count.



OP	Data
LD	0100
LD	0101
CNT	001
✳	00
LD-CNT	001
OUT	0050

- CNT001 operates for 814 counts according to the data of the external setting device shown in the above figure.
- When ✳ is entered into the count setting area, external count setting is specified.
- For example, when ✳00 is entered, relay Nos. 0000 ~ 0007 and 0010 ~ 0013 are assigned as the external terminals for external setting.
  Also, when ✳02 is entered, relay Nos. 0030 ~ 0033 are assigned as the external terminals.

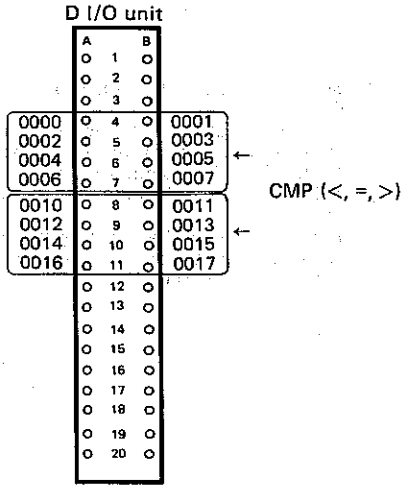
■ WHEN FAL INSTRUCTION IS USED



OP	Data	
LD	0000	
OR	0050	
AND·NOT	0001	
OUT	0050	
TIM	000	
	100	
LD	0050	
AND·TIM	000	
FAL	01	*
LD	0002	
FAL	00	**

NOTES:
* In the left figure, the ON time of output relay 0050 is monitored. If the ON time of output relay 0050 is less than 10sec, the relay operation is normal. If the ON time exceeds 10sec for some reason or other, the failure or abnormal mode (01) is output to special auxiliary relay Nos. 1340 ~ 1347.
** To reset special auxiliary relay Nos. 1340 ~ 1347, execute the FAL00 instruction and the logical state of all the relays will become "0."

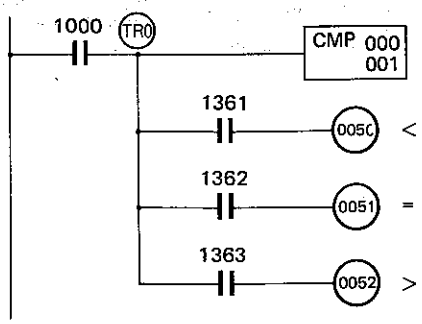
■ WHEN CMP INSTRUCTION IS USED



Result → Less than (<) — Special auxiliary relay No. 1361 operates.

Equal (=) — Special auxiliary relay No. 1362 operates.

Greater than (>) — Special auxiliary relay No. 1363 operates.

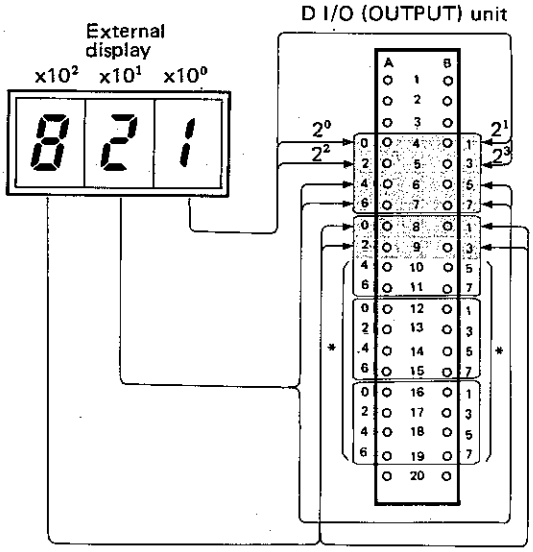


OP	Data
LD	1000
OUT·TR	0
CMP	000
	001
LD·TR	0
AND	1361
OUT	0050
LD·TR	0
AND	1362
OUT	0051
LD·TR	0
AND	1363
OUT	0052

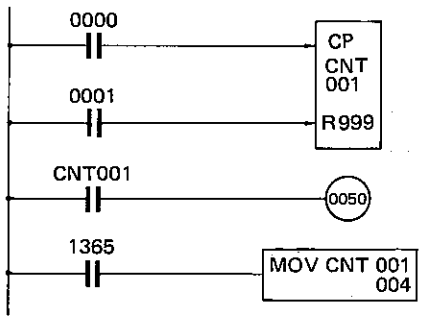
- The numeric data 000 and 001 of the CMP instruction are used by cutting the low-order digit (0 ~ 7) of relay Nos. 0000 ~ 0007 and 0010 ~ 0017, respectively.
- In the left figure, the 8 bits of relay Nos. 0000 ~ 0007 are compared with the 8 bits of relay Nos. 0010 ~ 0017 when relay No. 1000 is ON and the result of the comparison is output to special auxiliary relay No. 1361, 1362, or 1363.
- Since the result of the CMP instruction execution is retained in the memory until the execution of the next CMP instruction or END instruction, be sure to insert the condition of the CMP instruction execution in series with the result of the comparison (special auxiliary relay Nos. 1361 ~ 1363).

■ WHEN MOV INSTRUCTIONS ARE USED

1. To externally display the counter data



NOTE: * This area can be used for other inputs

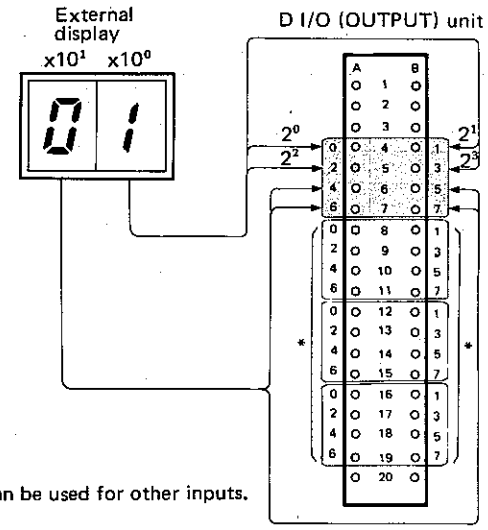


OP	Data
LD	0000
LD	0001
CNT	001
	999
LD-CNT	001
OUT	0050
LD	1365
MOV-CNT	001
	004 *

- By connecting an external 3-digit display to output relay Nos. 0040 ~ 0053, the changing data of the counter is indicated on the external display.
- Since the counter is of a decrementing type, the external dispaly indicates the remaining counts.

- Special auxiliary relay No. 1365 is normally ON.
- * mark indicates the location to which data is to be transferred by the MOV instruction. (Data 004 indicates external terminals 0040 ~ 0053 to which the data is to be transferred.)
- In the left figure, the changing data CNT001 is indicated on the external display through external terminals 0040 ~ 0053.

2. To externally display the diagnostic (FAL) result



NOTE: * This area can be used for other inputs.

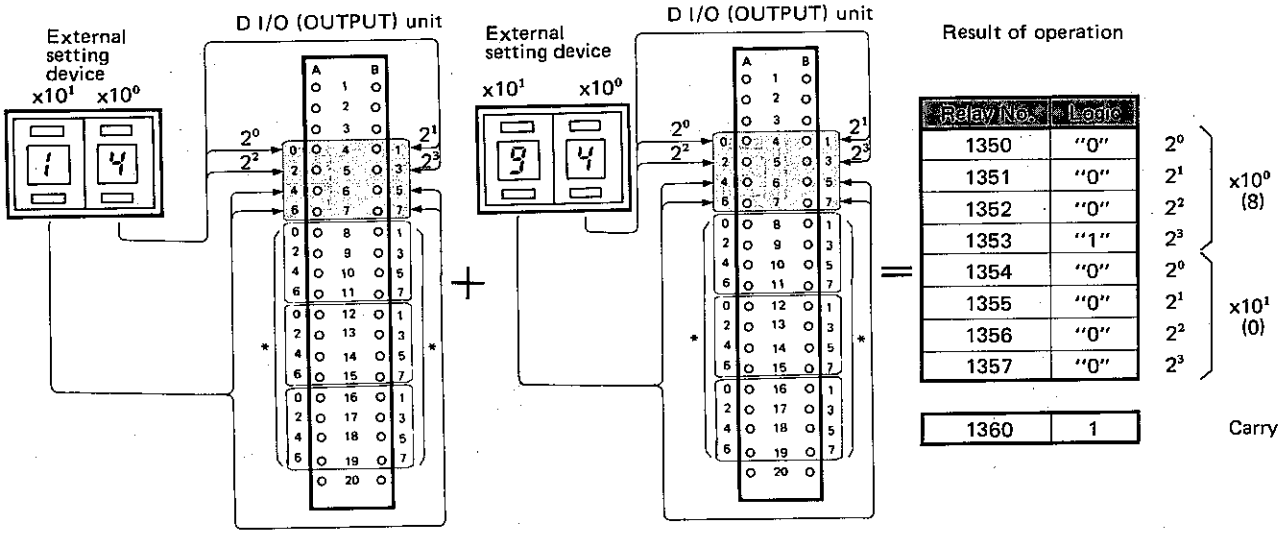
OP	Data
LD	1365
MOV	134
	005

- By connecting an external 2-digit display to output relay Nos. 0050 ~ 0057, the failure or abnormal mode (01 ~ 99) is indicated on the external display.

- Relay No. 1365 is normally in the ON state.
- The numeric data 134 and 005 of the MOV instruction are used by cutting the low-order digit (0 ~ 7) of relay Nos. 0050 ~ 0057 (FAL data).
- In the left figure, the 8 bits data of special auxiliary relay Nos. 1340 ~ 1347 are transferred to the 8 bits of the relay Nos. 0050 ~ 0057 and indicated on the external display.

■ WHEN ADD (+) INSTRUCTION IS USED

1. To add one externally set data to the other externally set data



Relay No.	Logic	
1350	"0"	2^0
1351	"0"	2^1
1352	"0"	2^2
1353	"1"	2^3
1354	"0"	2^0
1355	"0"	2^1
1356	"0"	2^2
1357	"0"	2^3

$x10^0$ (8)

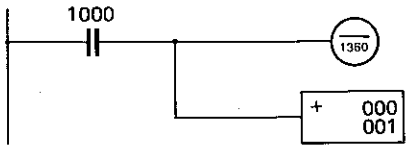
$x10^1$ (0)

1360	1

Carry

NOTE: * This area can be used for other inputs.

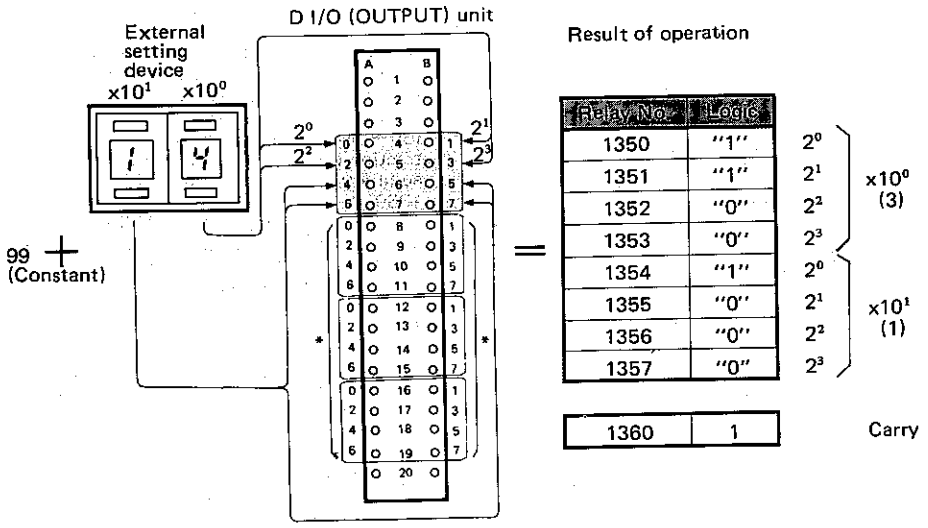
NOTE: * This area can be used for other inputs.



OP	Data
LD	1000
OUT·NOT	1360
+	000
	001

- By connecting an external 2-digit setting device to input relay Nos. 0000 ~ 0007 and 0010 ~ 0017, respectively, the data set by both the external setting devices are added together and the result of the addition is output in BCD to special auxiliary relay Nos. 1350 ~ 1357 and 1360.
- The OUT NOT instruction (1360) is for initial resetting of special auxiliary relay No. 1360 and this instruction must always be used immediately before the ADD (+) instruction.
- The numeric data 000 and 001 of the ADD (+) instruction are used by cutting the low-order digit (0 ~ 7) of relay Nos. 0000 ~ 0007 and 0010 ~ 0017, respectively.
- In the left figure, the data "14" and "94" of both the external setting devices when relay No. 1000 is ON are added and the result of the addition "08" which represents the last 2 digits of "108" is output to special auxiliary relay Nos. 1350 ~ 1357.
  At the same time, special auxiliary relay No. 1360 (Carry) operates, indicating that a carry exists in the result.

2. To add fixed data to externally set data



Relay No.	Logic	
1350	"1"	2^0
1351	"1"	2^1
1352	"0"	2^2
1353	"0"	2^3
1354	"1"	2^0
1355	"0"	2^1
1356	"0"	2^2
1357	"0"	2^3

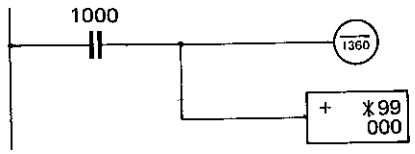
$x10^0$ (3)

$x10^1$ (1)

1360	1

Carry

NOTE: * This area can be used for other inputs.

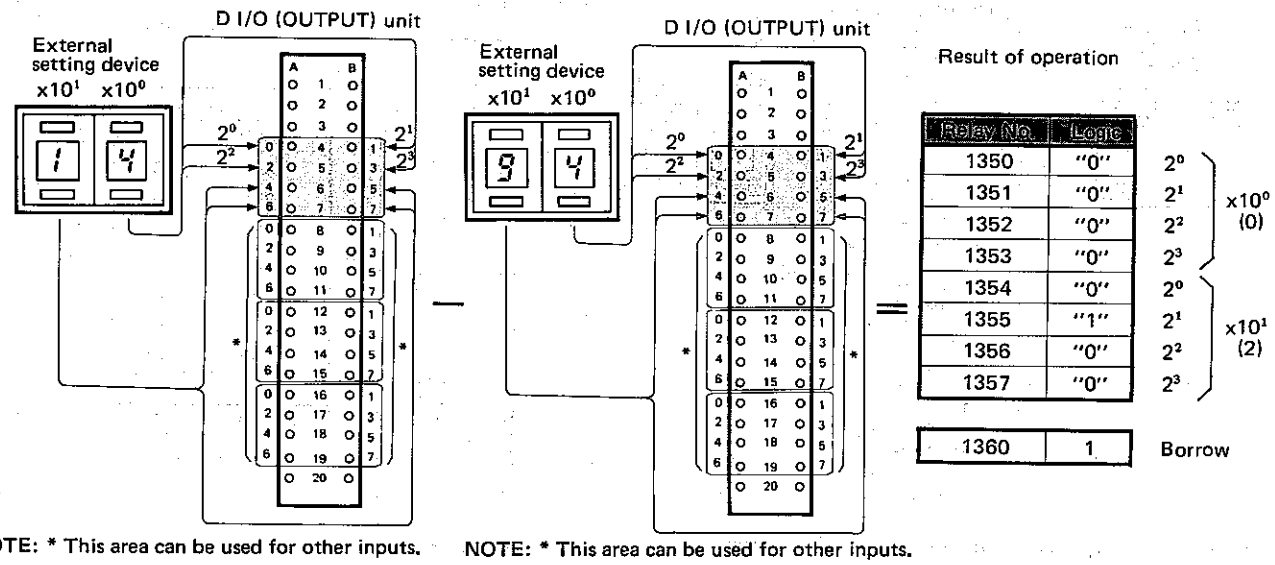


OP	Data
LD	1000
OUT·NOT	1360
+✱	99
	000

- By connecting an external 2-digit setting device to input relay Nos. 0000 ~ 0007, the constant (00 ~ 99) is added to the data set by the external setting device and the result of the addition is output in BCD to special auxiliary relay Nos. 1350 ~ 1357 and 1360.
- The OUT NOT instruction (1360) is for initial resetting of special auxiliary relay No. 1360 and this instruction must always be used immediately before the ADD (+) instruction.
- The data ✱99 of the ADD (+) instruction indicates the fixed data and the data 000 is used by cutting the low-order digit (0 ~ 7) of the relay Nos. 0000 ~ 0007.
- In the left figure, the constant "99" is added to the externally set data "14" when relay No. 1000 is ON and the result of the addition "13" which represents the last 2 digits "113" is output to special auxiliary relay Nos. 1350 ~ 1357. At the same time, special auxiliary relay No. 1360 (Carry) operates, indicating that a carry exists in the result.

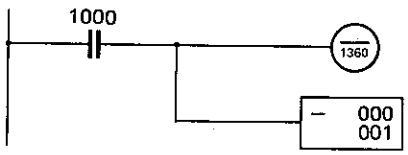
■ WHEN SUB (—) INSTRUCTIONS ARE USED

1. To subtract one externally set data from the other externally set data.



NOTE: * This area can be used for other inputs.

NOTE: * This area can be used for other inputs.



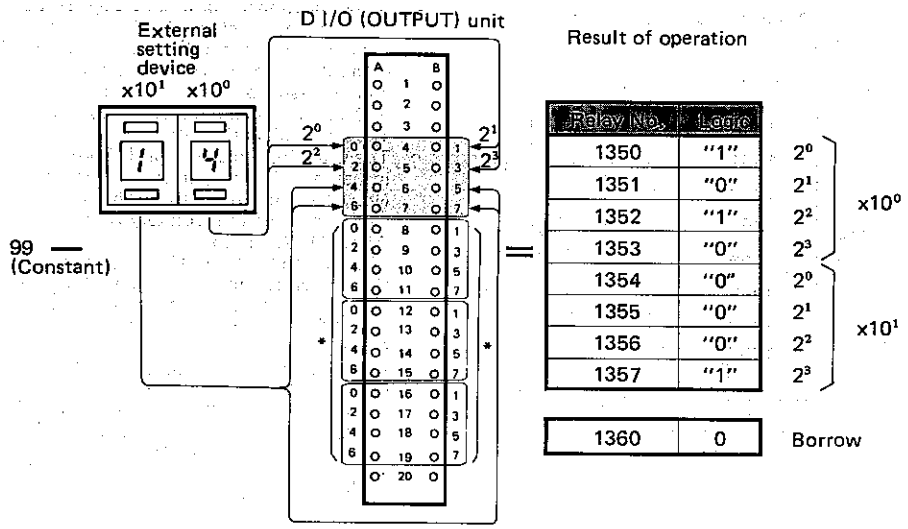
OP	Data
LD	1000
OUT·NOT	1360
—	000
	001

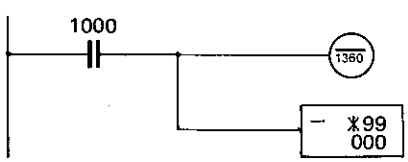
- By connecting an external 2-digit setting device to input relay Nos. 0000 ~ 0007 and 0010 ~ 0017, respectively, the data set by one externally setting device is subtracted from the data set by the other external setting device and the result of the subtraction is output in BCD to special auxiliary relay Nos. 1350 ~ 1357 and 1360.
- The OUT NOT instruction (1360) is for initial resetting of special auxiliary relay No. 1360 and this instruction must always be used immediately before the SUB (—) instruction.
- The data 000 and 001 of the SUB (—) instruction are used by cutting the low-order digits (0 ~ 7) of relay Nos. 0000 ~ 0007 and 0010 ~ 0017, respectively.
- In the left figure, one externally set data "94" is subtracted from the other externally set data "14" when relay No. 1000 is ON and the result of the subtraction "20" is output to special auxiliary relay Nos. 1350 ~ 1357. At the same time, special auxiliary relay No. 1360 (Borrow) operates indicating that the result is a complement. To obtain a true complement, the complement must be subtracted from 00.

  00 — 20 = —80

  The data "80" is then output to special auxiliary relay Nos. 1350 ~ 1357 and special auxiliary relay No. 1360 operates.

2. To subtract externally set data from fixed data.



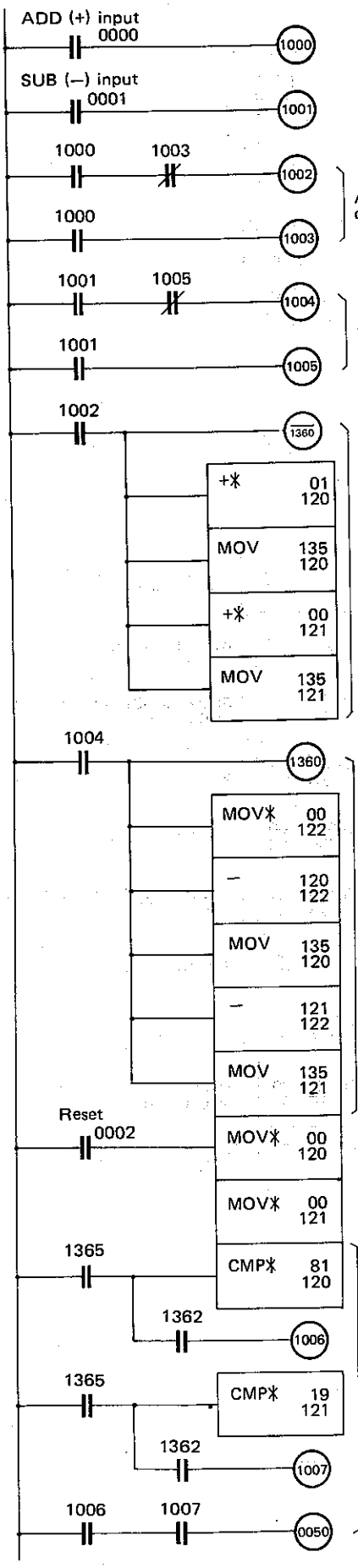


OP	Data
LD	1000
OUT·NOT	1360
—⁑	99
	000

- By connecting an external 2-digit setting device to input relay Nos. 0000 ~ 0007, the data set by the external setting device is subtracted from the constant (00 ~ 99) and the result of the subtraction is output in BCD to special auxiliary relay Nos. 1350 ~ 1357 and 1360.
- The OUT NOT instruction (1360) is for initial resetting of special auxiliary relay No. 1360 and this instruction must always be used immediately before the SUB (—) instruction.
- The data ⁑99 of the SUB (—) instruction indicates the fixed data and the data 000 is used by cutting the low-order digit (0 ~ 7) of relay Nos. 0000 ~ 0007.
- In the left figure, the data "14" of the external setting device is subtracted from the constant 99 when the relay No. 1000 is ON and the result of the subtraction "85" is output to special auxiliary relay Nos. 1350 ~ 1357. Special auxiliary relay No. 1360 (Borrow) releases, indicating that the result is a true complement.

■ EXAMPLE OF ADD (+)/SUB (–) COUNTER CIRCUIT

1. Decimal 4-digit reversible counter



Calculation result area (Special auxiliary relays)

1360	1357	1356	1355	1354	1353	1352	1351	1350
Carry Borrow	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
	$\times 10^1$ (High-order digit)				$\times 10^0$ (Low-order digit)			

Work area (Internal auxiliary relays)

1207	1206	1205	1204	1203	1202	1201	1200
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
$\times 10^1$				$\times 10^0$ (Low-order digit)			

1217	1216	1215	1214	1213	1212	1211	1210
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
$\times 10^3$ (High-order digit)				$\times 10^2$			

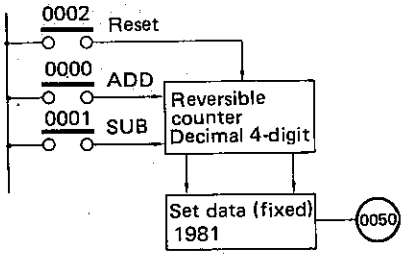
Data area (Internal auxiliary relays)

1227	1226	1225	1224	1223	1222	1221	1220
"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"
$\times 10^1$ (High-order digit)				$\times 10^0$ (Low-order digit)			

OP	Data
LD	0000
OUT	1000
LD	0001
OUT	1001
LD	1000
AND-NOT	1003
OUT	1002
LD	1000
OUT	1003
LD	1001
AND-NOT	1005
OUT	1004
LD	1001
OUT	1005
LD	1002
OUT-NOT	1360
+·✳	01
	120
MOV	135
	120
+·✳	00
	121
MOV	135
	121
LD	1004
OUT	1360
MOV·✳	00
	122
–	120
	122
MOV	135
	120
–	121
	122
MOV	135
	121

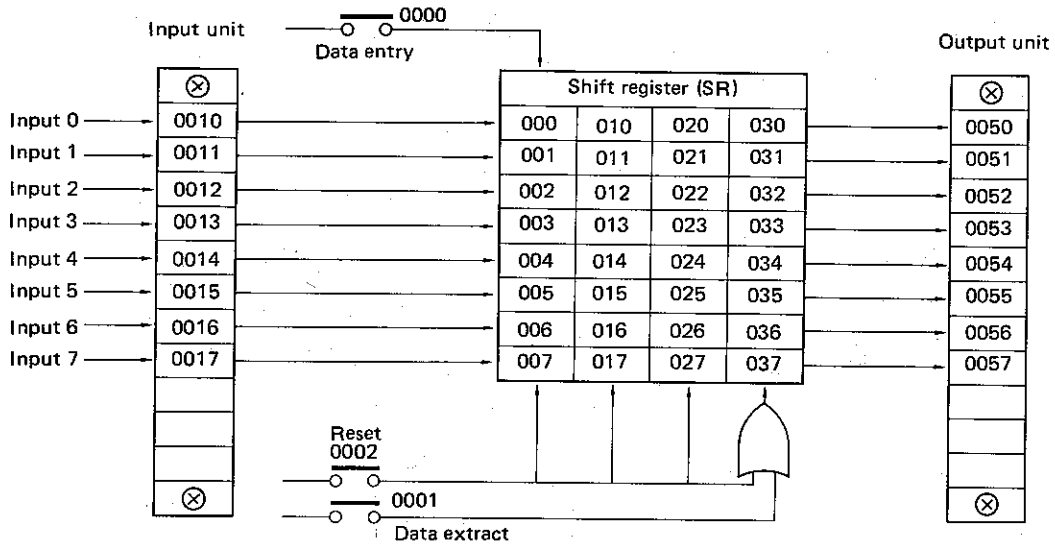
OP	Data
LD	0002
MOV·✳	00
	120
MOV·✳	00
	121
LD	1365
CMP·✳	81
	120
AND	1362
OUT	1006
LD	1365
CMP·✳	19
	121
AND	1362
OUT	1007
LD	1006
AND	1007
OUT	0050

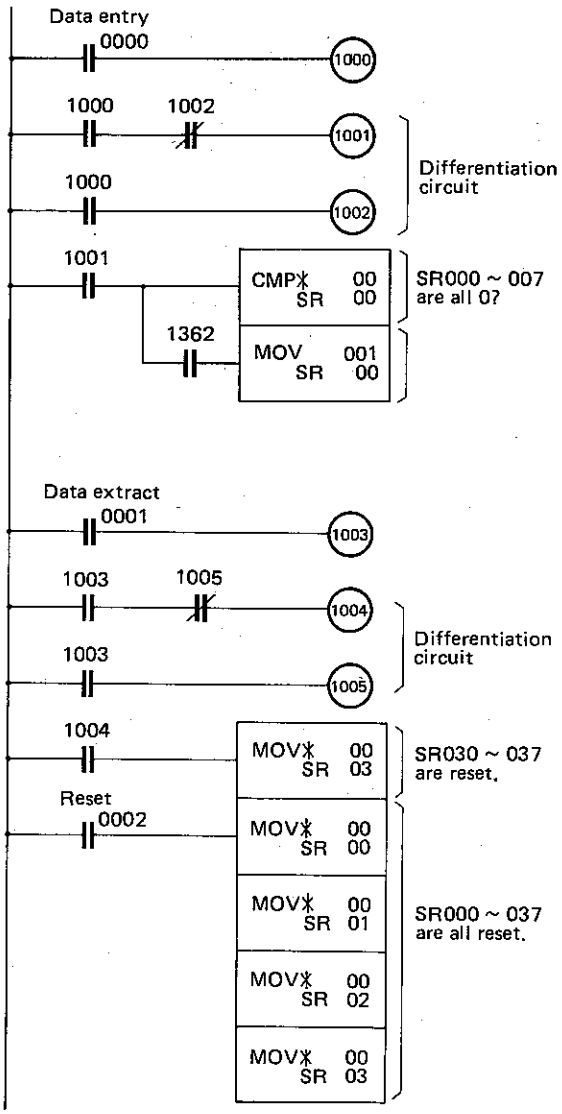
- Special auxiliary relay No. 1365 is normally ON.
- Special auxiliary relay No. 1362 operates when the result of the CMP instruction is equal (=).
- Equivalence circuit

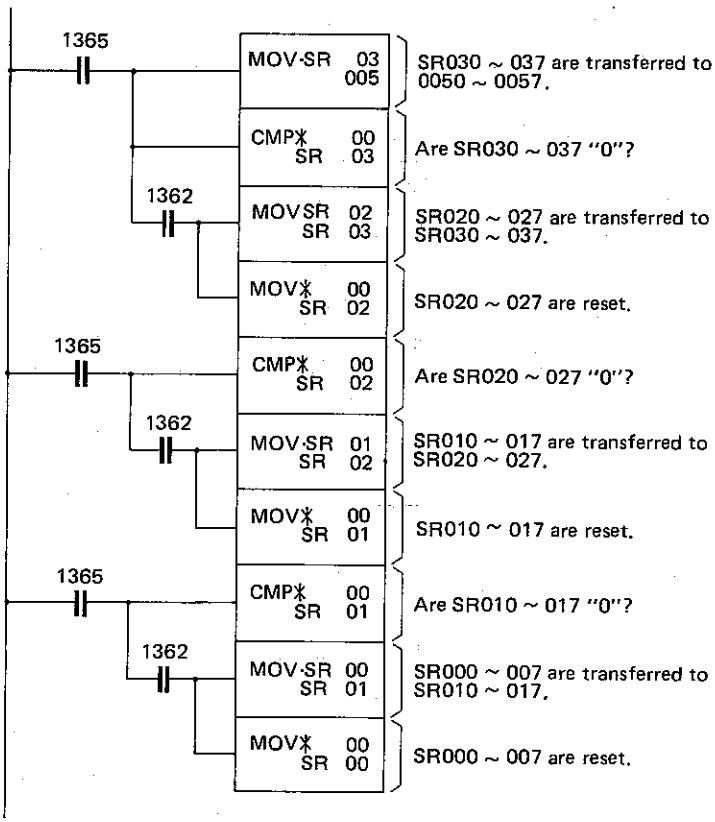


- If it is desired to retain the count data in the memory at the time of a power failure, use a latching relay and a shift register in the work area. In this manner, the data can be retained until a reset signal is input.

■ 8-BIT 4-STAGE FIFO SHIFT REGISTER





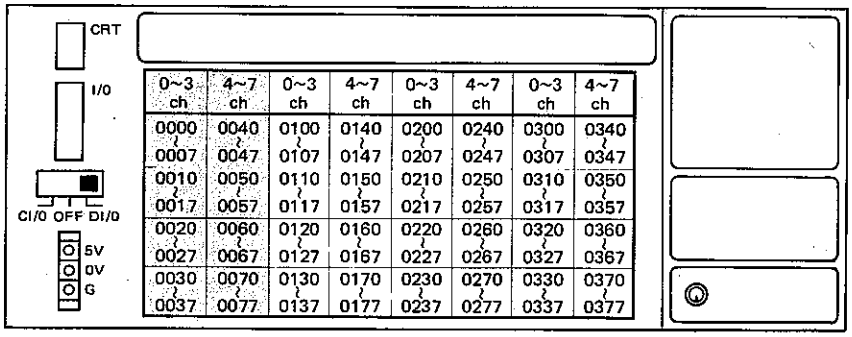


OP	Data
LD	0000
OUT	1000
LD	1000
AND·NOT	1002
OUT	1001
LD	1000
OUT	1002
LD	1001
CMP·✳	00
SR	00
AND	1362
MOV	001
SR	00
LD	0001
OUT	1003
LD	1003
AND·NOT	1005
OUT	1004
LD	1003
OUT	1005
LD	1004
MOV·✳	00
SR	03
LD	0002
MOV·✳	00
SR	00
MOV·✳	00
SR	01
MOV·✳	00
SR	02
MOV·✳	00
SR	03
LD	1365
MOV·SR	03
	005
CMP·✳	00
SR	03
AND	1362
MOV·SR	02
SR	03
MOV·✳	00
SR	02
LD	1365
CMP·✳	00
SR	02
AND	1362
MOV·SR	01
SR	02
MOV·✳	00
SR	01
LD	1365
CMP·✳	00
SR	01
AND	1362
MOV·SR	00
SR	01
MOV·✳	00
SR	00

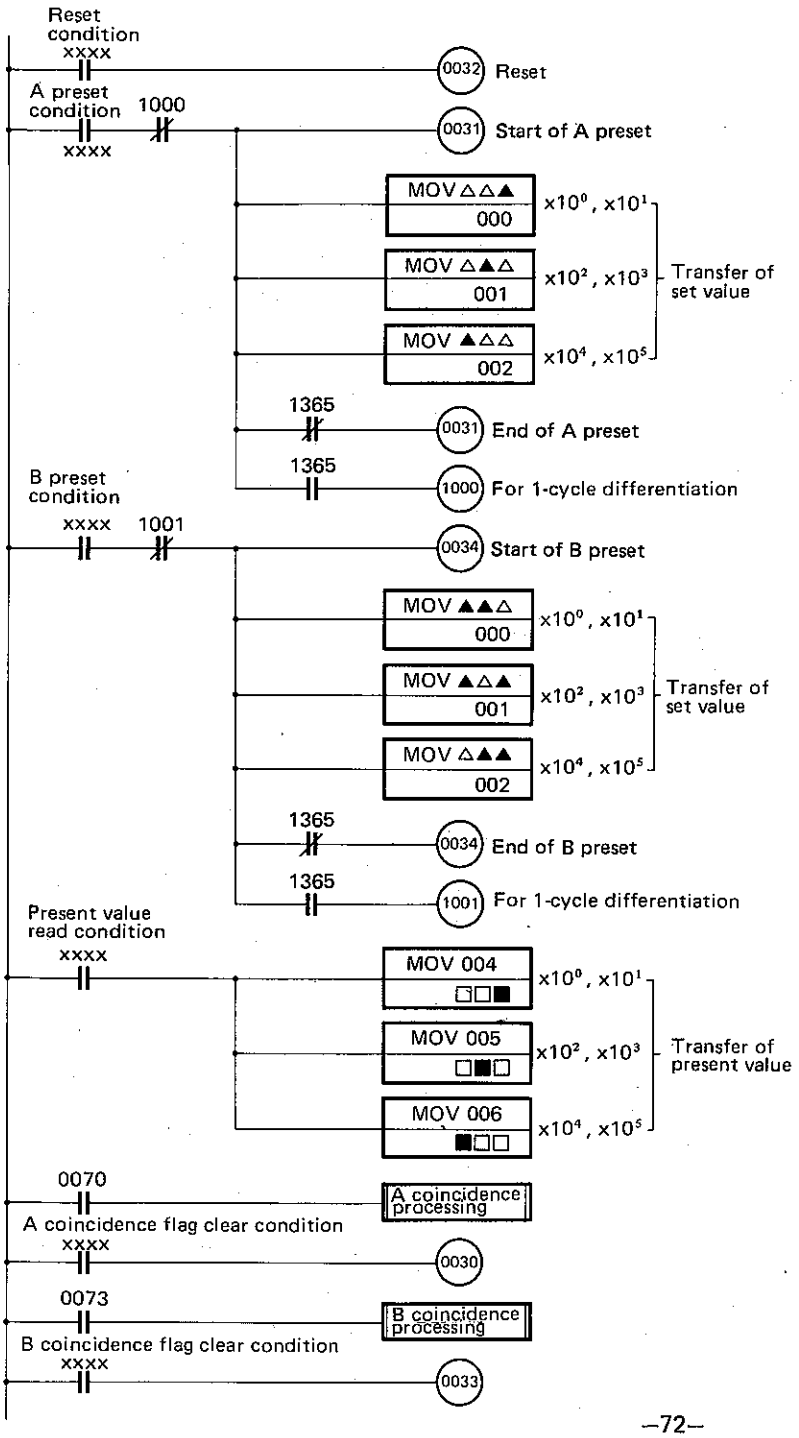
- Special auxiliary relay No. 1365 is normally ON.
- Special auxiliary relay No. 1362 operates when the result of the CMP instruction execution is equal (=).
- Shift data is retained in the memory at the time of a power failure.

■ PROGRAMMING EXAMPLE OF HIGH-SPEED COUNTER UNIT

Illustrated below is a programming example when a high-speed counter unit is inserted to the positions indicated in the figure below on the CPU rack whose C I/O, D I/O selector switch is set to the "D I/O" position.



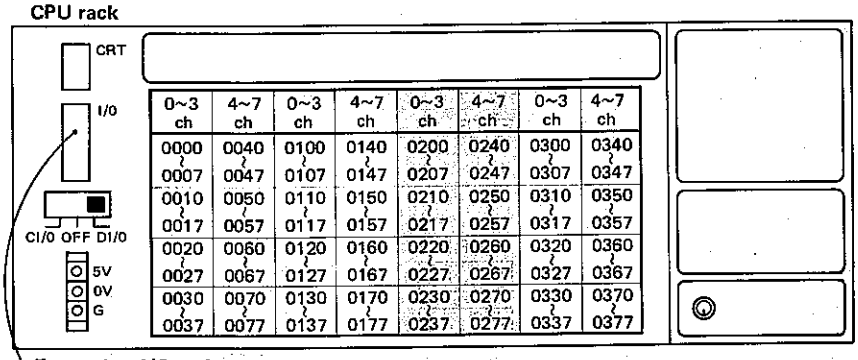
0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0000 ~ 0007	0040 ~ 0047	0100 ~ 0107	0140 ~ 0147	0200 ~ 0207	0240 ~ 0247	0300 ~ 0307	0340 ~ 0347
0010 ~ 0017	0050 ~ 0057	0110 ~ 0117	0150 ~ 0157	0210 ~ 0217	0250 ~ 0257	0310 ~ 0317	0350 ~ 0357
0020 ~ 0027	0060 ~ 0067	0120 ~ 0127	0160 ~ 0167	0220 ~ 0227	0260 ~ 0267	0320 ~ 0327	0360 ~ 0367
0030 ~ 0037	0070 ~ 0077	0130 ~ 0137	0170 ~ 0177	0230 ~ 0237	0270 ~ 0277	0330 ~ 0337	0370 ~ 0377



■ PROGRAMMING EXAMPLE OF D/A CONVERSION UNIT

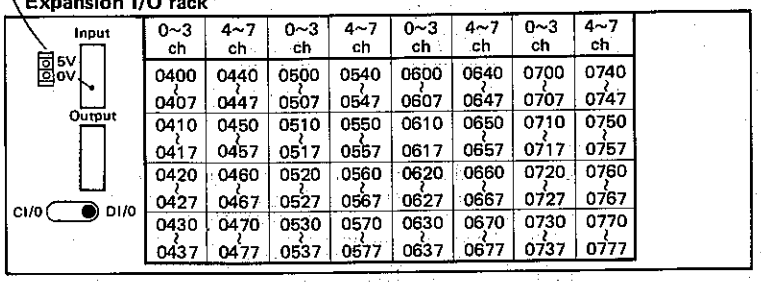
Illustrated below is a programming example when a D/A conversion unit is inserted to the positions indicated below on the CPU rack whose C I/O, D I/O selector switch is set to the "D I/O" position.

CPU rack

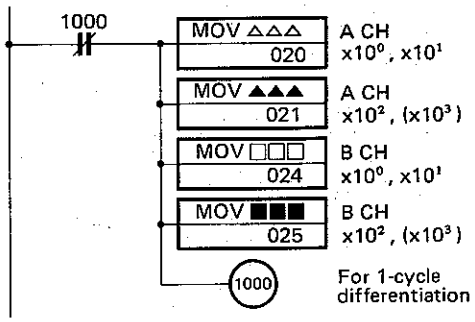


0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0000 ~ 0007	0040 ~ 0047	0100 ~ 0107	0140 ~ 0147	0200 ~ 0207	0240 ~ 0247	0300 ~ 0307	0340 ~ 0347
0010 ~ 0017	0050 ~ 0057	0110 ~ 0117	0150 ~ 0157	0210 ~ 0217	0250 ~ 0257	0310 ~ 0317	0350 ~ 0357
0020 ~ 0027	0060 ~ 0067	0120 ~ 0127	0160 ~ 0167	0220 ~ 0227	0260 ~ 0267	0320 ~ 0327	0360 ~ 0367
0030 ~ 0037	0070 ~ 0077	0130 ~ 0137	0170 ~ 0177	0230 ~ 0237	0270 ~ 0277	0330 ~ 0337	0370 ~ 0377

Expansion I/O rack



0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0400 ~ 0407	0440 ~ 0447	0500 ~ 0507	0540 ~ 0547	0600 ~ 0607	0640 ~ 0647	0700 ~ 0707	0740 ~ 0747
0410 ~ 0417	0450 ~ 0457	0510 ~ 0517	0550 ~ 0557	0610 ~ 0617	0650 ~ 0657	0710 ~ 0717	0750 ~ 0757
0420 ~ 0427	0460 ~ 0467	0520 ~ 0527	0560 ~ 0567	0620 ~ 0627	0660 ~ 0667	0720 ~ 0727	0760 ~ 0767
0430 ~ 0437	0470 ~ 0477	0530 ~ 0537	0570 ~ 0577	0630 ~ 0637	0670 ~ 0677	0730 ~ 0737	0770 ~ 0777

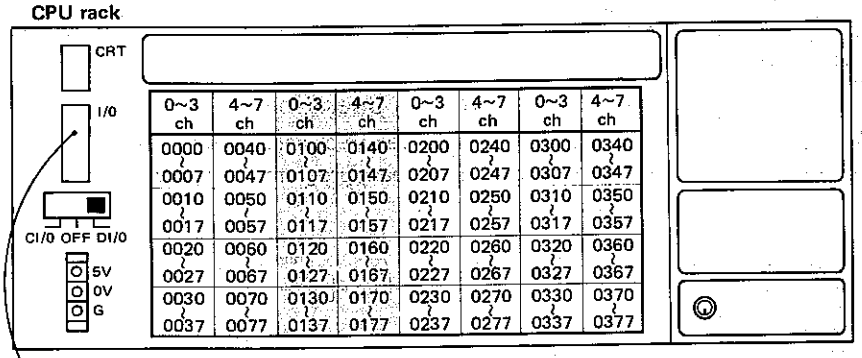


- Data △△△ or □□□ are output to the D/A converter using program scan.

■ PROGRAMMING EXAMPLE OF A/D CONVERSION UNIT

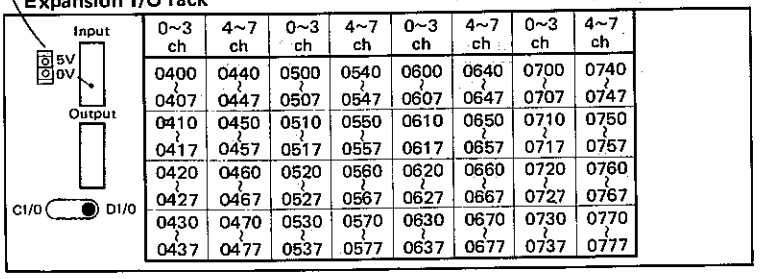
Illustrated below is a programming example when an A/D conversion unit is inserted to the positions indicated below on the CPU rack whose C I/O, D I/O selector switch is set to the "D I/O" position.

CPU rack

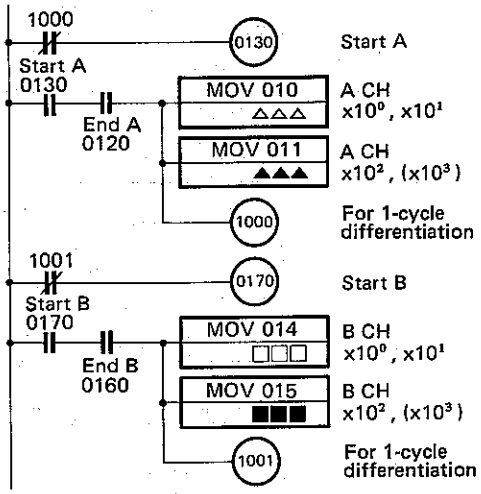


0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0000 ~ 0007	0040 ~ 0047	0100 ~ 0107	0140 ~ 0147	0200 ~ 0207	0240 ~ 0247	0300 ~ 0307	0340 ~ 0347
0010 ~ 0017	0050 ~ 0057	0110 ~ 0117	0150 ~ 0157	0210 ~ 0217	0250 ~ 0257	0310 ~ 0317	0350 ~ 0357
0020 ~ 0027	0060 ~ 0067	0120 ~ 0127	0160 ~ 0167	0220 ~ 0227	0260 ~ 0267	0320 ~ 0327	0360 ~ 0367
0030 ~ 0037	0070 ~ 0077	0130 ~ 0137	0170 ~ 0177	0230 ~ 0237	0270 ~ 0277	0330 ~ 0337	0370 ~ 0377

Expansion I/O rack



0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch	0~3 ch	4~7 ch
0400 ~ 0407	0440 ~ 0447	0500 ~ 0507	0540 ~ 0547	0600 ~ 0607	0640 ~ 0647	0700 ~ 0707	0740 ~ 0747
0410 ~ 0417	0450 ~ 0457	0510 ~ 0517	0550 ~ 0557	0610 ~ 0617	0650 ~ 0657	0710 ~ 0717	0750 ~ 0757
0420 ~ 0427	0460 ~ 0467	0520 ~ 0527	0560 ~ 0567	0620 ~ 0627	0660 ~ 0667	0720 ~ 0727	0760 ~ 0767
0430 ~ 0437	0470 ~ 0477	0530 ~ 0537	0570 ~ 0577	0630 ~ 0637	0670 ~ 0677	0730 ~ 0737	0770 ~ 0777



- Data from the A/D converter is fetched into △△△ or □□□ using program scan.

6. Operating Procedure

6.1 Cautions in Operating SYSMAC-M1R

When operating the SYSMAC-M1R, pay attention to the following points.

CAUTIONS:
- **Before mounting I/O units in the CPU rack or before making connections, be sure turn off the AC power being supplied to the SYSMAC-M1R or set the Power switch (factory-set to the "ON" position prior to shipment) of the SYSMAC-M1R to the "OFF" position.**
- **Before power application, be sure to set the desired supply voltage using the voltage selector switch. (The rated voltage is factory-set to AC 240V prior to shipment.)**
- **Be sure to set the C I/O, D I/O selector switch and RAM/ROM selector switch properly. (Prior to shipment, the C I/O, D I/O selector switch is factory-set to the "C I/O" position and the RAM/ROM selector switch to the "RAM" position.**

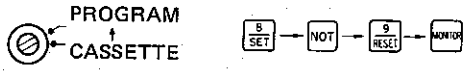
6.2 Basic Functions

Items of Operation	Description
All program clear	Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.
Address setting	Address setting is required to designate an address in such operations as program read, program write, etc.
Program write	This operation is to store a program in the specified memory address.
Program read	This operation is to confirm whether or not data has been programmed properly in the specified memory address.
Program check	This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).
RUN	This operation is to place the SYSMAC-M1R in the RUN (Program Execution) state.
Monitor	This operation is to monitor and display operating state of each relay, the operating state of each bit in the shift register or latching relay, or the present value of each timer or counter during execution of a program.
Multi monitor	This operation is to monitor and display the operating state of each relay, the operating state of each bit in the shift register or latching relay, or the present value of a timer or counter during the execution of a program.
Trace (continuity) check	When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.
Forced set/reset	This operation is to set or reset by force the operating state of a latching relay, the operating state of each bit in the shift register and the present value of a timer or counter during the execution of a program.
Instruction search	When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction has been written in a program to be searched.
Contact (coil) number change	This operation is to change contact (or coil) number(s) in a program due to a circuit modification.
Contact (coil) addition	This operation is employed when contact (or coil) number(s) is to be added due to a circuit modification.
Contact (coil) deletion	This operation is to change contact (coil) number(s) from a program due to a circuit modification.

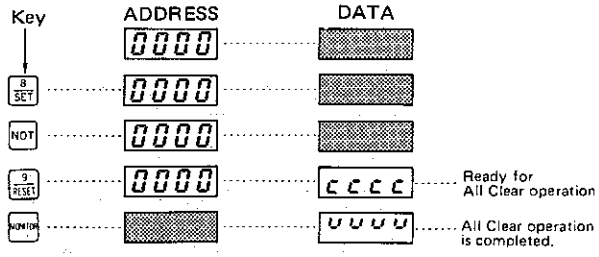
6.3 All Program Clear Operation

Since the CPU retains previously stored data (of SR, KR and CNT) in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.

- **Operating procedure**



- **Display**



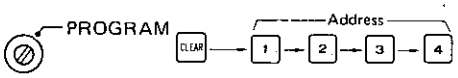
NOTES:
1. By the All Clear operation, all the programs (I/O relays, internal auxiliary relays, latching relays, timers and counters) stored in addresses 0000 ~ 3999 are cleared.
2. Before the key operation, change the mode selector switch position from "CASSETTE" to "PROGRAM."
3. In the All Clear operation, a beep sound is generated at the depression of each key.
4. Upon depression of the MONITOR key, the ADDRESS display is extinguished. Subsequent depression of the CLEAR key will cause the ADDRESS display to indicate "0000."

CAUTION:
After the PROGRAM mode selection, depression of the CLEAR key or any key other than the four keys shown above will not allow All Clear operation to be executed. In this case, repeat the operation starting from the mode selection.

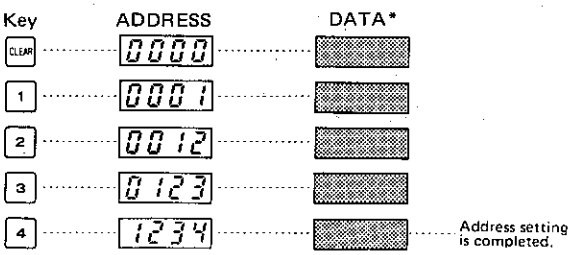
6.4 Address Setting Operation

Address setting is required to designate an address in such operations as program read, program write, etc.

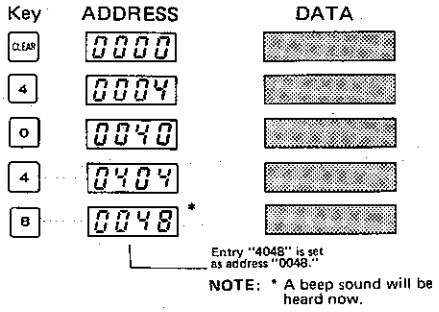
- **Operating procedure**



- **Display**



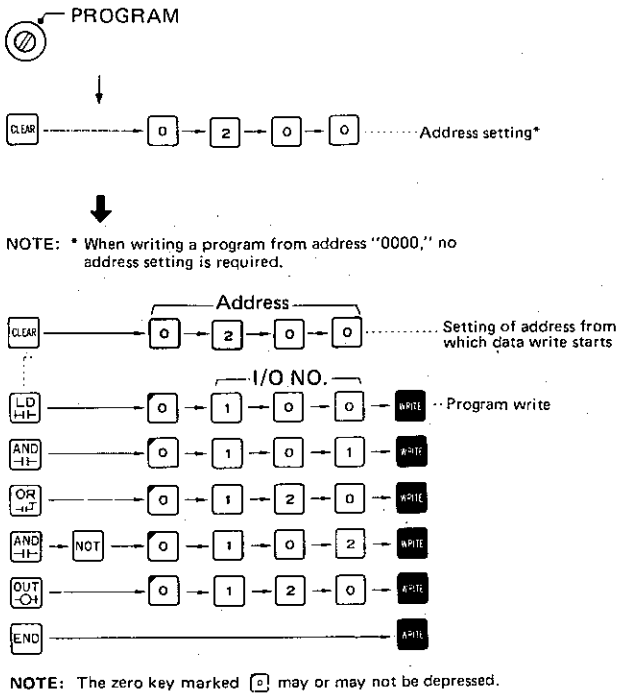
NOTES:
1. Each address is set in 4 digits using numeric 0000 ~ 3999. To set address "0000," no numeric entry is required. To set address "0003," depress only numeric key [3] and to set address "0023," depress only numeric keys [2] and [3]. Preceding zero(s) may be omitted from key entry.
2. * The data entered will not be displayed by the address setting operation alone. To display the data entered, [↑] [↓] keys must be depressed.
3. In address setting, when numeric data entered as an address exceeds 3999, the first two digits of the 4-digit address are automatically processed as "0." Since the CPU does not recognize this as an error, the only way to identify this error is through confirmation by the operator. For example, if address 4048 is entered, it will be set as follows.



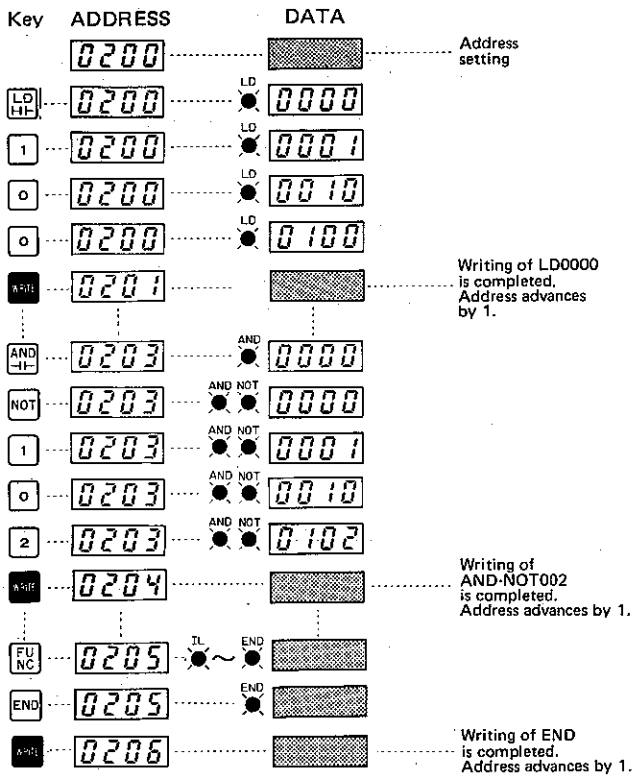
6.5 Program Write Operation

This operation is to store a program in the specified memory address.

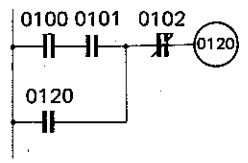
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	OR	0120
0203	AND-NOT	0102
0204	OUT	0120
0205	END	

NOTES:
1. At each depression of the WRITE key, the data appearing on the OP and DATA displays are written into memory.
2. When the WRITE key is depressed in the following cases, a beep sound is generated to signal an erroneous key operation.
   ① When the key is depressed in other than the PROGRAM mode.
   ② When a symbolic or numeric entry error exists (numeric entry error is applicable only when an SR instruction is used).
3. When the WRITE key is depressed in the following cases, a beep sound is generated to signal the requirement of a program change.
   ① When an overflow exists (no space for one word exists in the last address where changing a one-word instruction to a 2-word instruction).
   ② When attempt is made to write an instruction with more than 2-word length into the last address.
4. The END instruction is executed by depressing the [FUN] key and then the [END] key. Upon depression of the [FUN] key, the following indicators on the OP display will illuminate.

   IL ILC JNP JME MOV CMP + − FAL END

   When the END [END] key is then depressed, only the END indicator ● illuminates, indicating that the instruction word END has been selected.

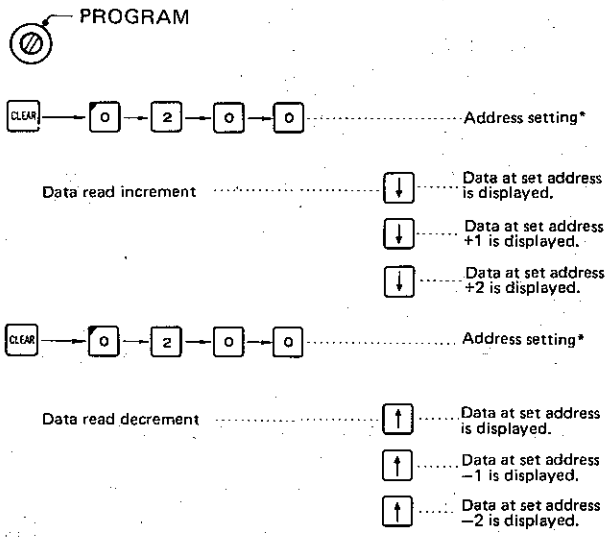
Correction Procedures when an error occurs in program write

1. If an error in programming is noticed before depressing the WRITE key, depress the CLEAR DISPLAY key and the re-entry operation becomes effective.
2. If an error in programming is discovered after depressing the WRITE key, repeat the operation from the address setting, or return to the address in which the error exists by depressing the ↑ key and then depress the CLEAR DISPLAY key and the re-entry operation becomes effective.

6.6 Program Read Operation

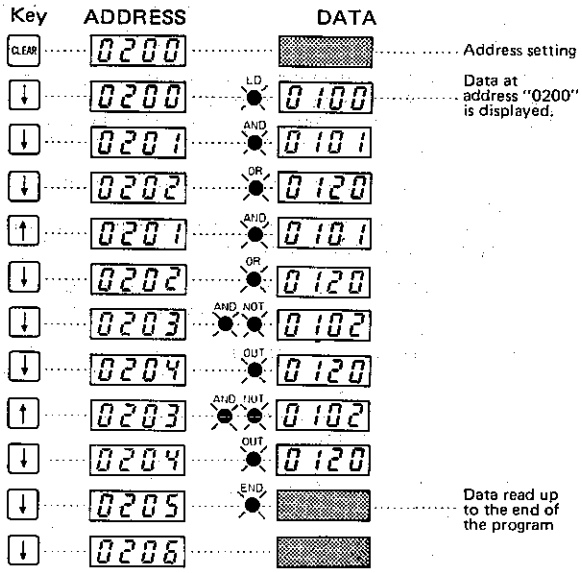
This operation is to confirm whether or not the data has been programmed properly in the specified memory address.

- **Operating procedure**

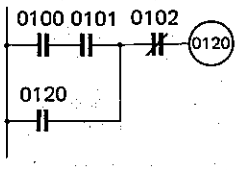


NOTES: 1. When reading a program from address "0000," no address setting is required.
2. The zero key marked 0 may or may not be depressed.

- **Display**



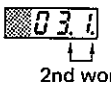
- **Circuit for exercise and programming example**



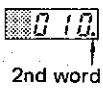
Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	OR	0120
0203	AND-NOT	0102
0204	OUT	0120
0205	END	

NOTES:
1. At each depression of the ↓ key, the data at the set address +1 is displayed (i.e., data read increment). However, when the address reaches 3999, a beep sound is generated at each depression of the ↓ key.
2. At each depression of the ↑ key, the data at the set address −1 is displayed (i.e., data read decrement). However, when the address reaches 0000, a beep sound is generated at each depression of the ↑ key.
3. In case of 2-word instructions, the 2nd word data is identified on the display as follows.

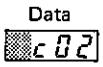
- MOV
  CMP
  ±



- SR



4. When TIM, CNT, MOV, CMP, + and − instructions are used, the data (✳02) are identified on the display as follows.



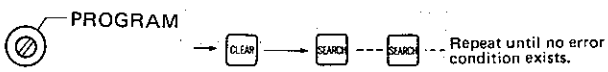
6.7 Program Check Operation

This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).

Items subject to program check are as follows.

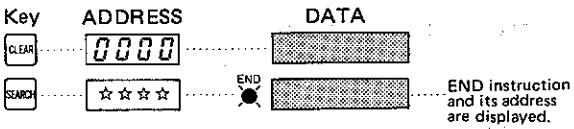
- Coil duplication error
- Circuit error
- IL/JMP error
- END instruction missing error

- **Operating procedure**

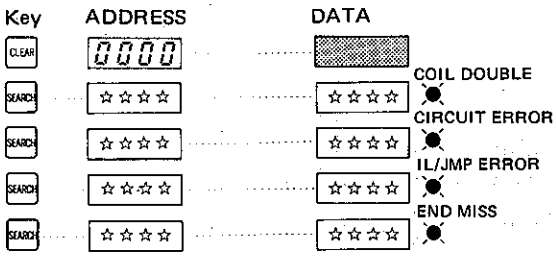


- **Display**

When a program error does not exist



When a program error exists



NOTE:
If a program error exists, the address where the error exists and its contents are displayed at each depression of the SEARCH key.

- **Error conditions**

1. Coil duplication error
   The "COIL DOUBLE" indicator illuminates when the OUT, OUT·NOT, OUT·SR, OUT·NOT·SR, SR, KR, TIM, CNT or MOV instructions of the same relay number except special auxiliary relays are contained in a program.
2. Circuit error
   The R register and S register are controlled by computing a difference between the number of logical start instructions (LD and LD·NOT) and the number of interblock logical instructions (AND·LD and OR·LD). If the difference is abnormal according to the nature of the instructions used when the result (OUT, OUT·NOT, OUT·SR, OUT·NOT·SR, CNT, TIM, SR, KR, FAL, CMP, MOV, MOV·NOT, +, −, IL, ILC, JMP, JME or END) is executed, it is regarded as a circuit error, and the "CIRCUIT ERROR" indicator illuminates.
3. IL/JMP error
   IL and ILC instructions and JMP and JME instructions must be used in pairs.
   When this rule is not observed in a program as shown below, "IL/JMP ERROR" indicator illuminates.
   ① ILC(JME) instruction is missing such as IL-IL (JMP-JMP).
   ② IL(JMP) instruction is missing and only ILC (JME) instruction is present.
   ③ The program ends with an IL (JMP) instruction before the END instruction or the last address.
4. END instruction missing error
   In the absence of an END instruction at the end of a program, the "END MISS" indicator illuminates.

NOTES:
1. If any programming error is discovered, correct the erroneous program in accordance with the program write procedure.
2. A circuit error is detected by taking that portion of the circuit from the LD-LD·NOT instruction after an OUT instruction to the next OUT instruction as a unit subject to detection.
3. Even if any of the following errors (except the END instruction missing error) occurs, the CPU can still perform the RUN operation. However, be sure to correct the error to execute the proper program.
   ① Coil duplication error
   ② Circuit error
   ③ IL/JMP error
4. Should an END instruction missing error occur, address 3998 is indicated as the last address on the ADDRESS display if the address contains a 2-word instruction. In all other cases, the last address is 3999.

6.8 RUN Operation

This operation is to place the SYSMAC-M1R in the RUN (Program Execution) condition.

- **Operating procedure**

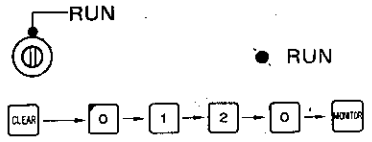
NOTES:
1. In the absence of an END instruction in a program, the RUN indicator will not illuminate even if the operation mode of the CPU is changed to "RUN." (All keys become inoperative.) At the same time, the "END MISS" indicator illuminates and the alarm buzzer sounds. In this case, change the operation mode to "PROGRAM" and enter an END instruction to correct the program.
2. After the CPU start operating, if an error occurs due to CPU failure or I/O bus failure, the RUN indicator goes out and the RUN outputs (control I/O relays) are turned off. All external outputs are also turned off.
   Refer to 9.4, LIST OF ERROR MESSAGES.
3. In other than the RUN mode, all external outputs are turned off. Also, when the "PROGRAM" mode is changed to the "RUN" mode, the CPU is initialized the same as when power is applied.

6.9 Monitor Operation

This operation is to monitor and display the operating state of each relay, the operating state of each bit in the shift register or latching relay, or the present value of each timer or counter during the execution of a program.

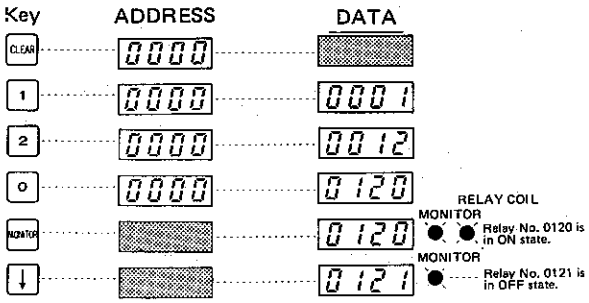
■ MONITORING OF THE OPERATING STATE OF AN INPUT/OUTPUT RELAY OR INTERNAL AUXILIARY RELAY

- **Operating procedure**



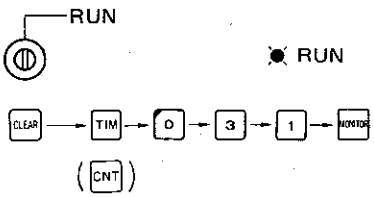
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**

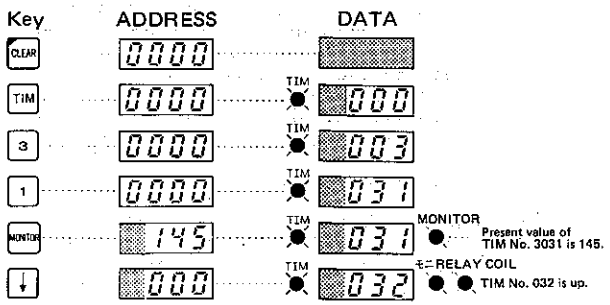


■ MONITORING OF THE PRESENT VALUE OF A TIMER OR COUNTER

- **Operating procedure**



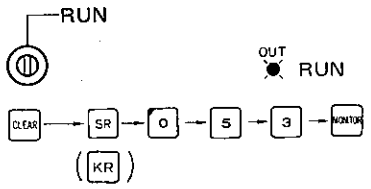
- **Display**



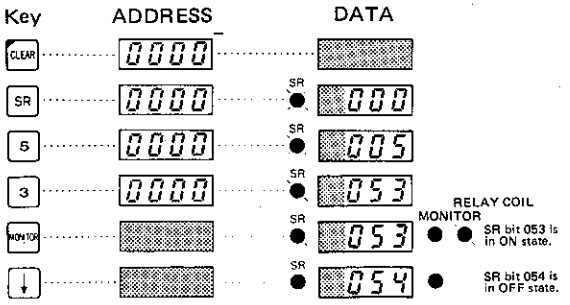
NOTE:
When the specified timer starts operating, the set time indicated on the ADDRESS display also starts to be decremented toward "0000," while indicating the present value (i.e., remaining time.).

■ MONITORING OF THE OPERATING STATE OF A SHIFT REGISTER OR LATCHING RELAY

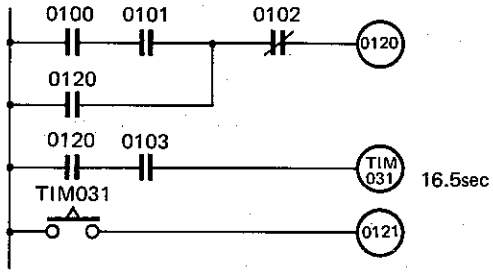
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



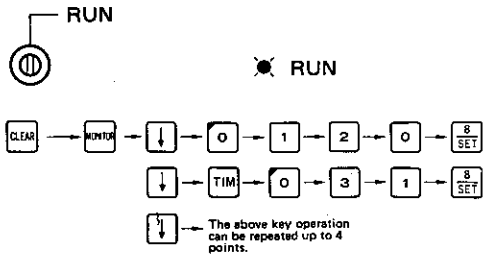
Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	OR	0120
0203	AND-NOT	0102
0204	OUT	0120
0205	LD	0120
0206	AND	0103
0207	TIM	031
0208		165
0209	LD-TIM	031
0210	OUT	0121
0211	END	

NOTES:
1. The operating state of each I/O relay, or internal auxiliary relay, is indicated by the "RELAY COIL" indicator (LED). This indicator illuminates when the state of the specified relay No. is ON and goes out when the state of the specified relay No. is OFF.
2. The present value of each timer or counter is indicated digitally on the ADDRESS display. When the set time of the specified timer has elapsed (or the set count of the specified counter is up), the "RELAY COIL" indicator illuminates.
3. The operating state of each bit in a shift register or latching relay is indicated by the "RELAY COIL" indicator. This indicator illuminates when the state of the specified bit number is ON and goes out when the state of the specified bit number is OFF.
4. Each depression of the ↓ or ↑ key subsequent to the depression of the MONITOR key causes a relay number, timer/counter number, or SR/KR bit number to be incremented or decremented by 1. Thus, the operating states of relays can be monitored consecutively.
5. When the MONITOR key is depressed in the following cases, a beep sound is generated to alert the operator. Check for the proper operating procedure.
   ① In other than RUN mode.
   ② When a symbolic or numeric error exists.
   ③ When an instruction other than OUT, OUT-NOT, OUT-NOT-SR, OUT-SR, TIM, CNT, SR and KR is used.
6. When the relay number reaches the upper limit during the monitor operation, each depression of the ↓ key causes a beep sound to be generated to alert the operator. Check for the proper operating procedure.
7. When the relay number becomes 0 during the monitor operation, each depression of the ↑ key causes a beep sound to be generated to alert the operator. Check for the proper operating procedure.

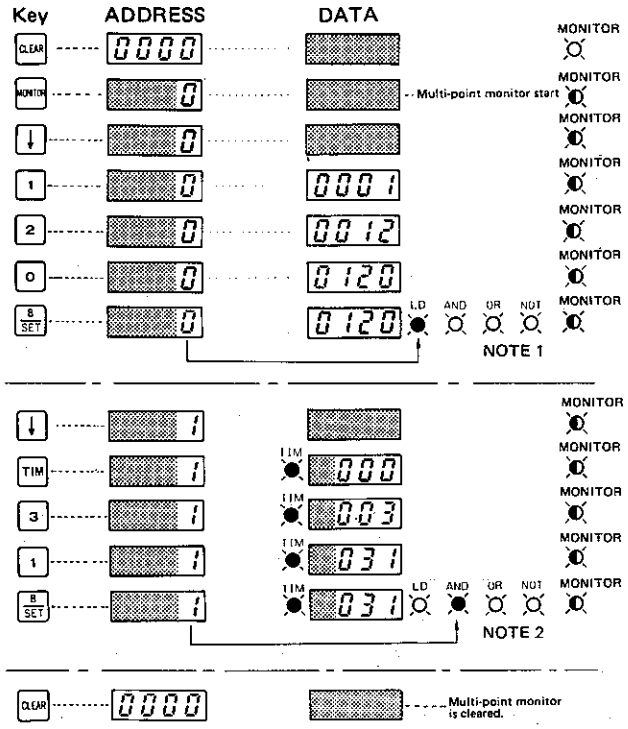
6.10 Multi Monitor Operation

This operation is simultaneously to monitor and display the operating states of a maximum of 4 relays, shift registers, latching relays, timers and/or counters during the execution of a program. However, for a timer or counter, only the time-up or count-up condition is monitored.

- **Operating procedure**



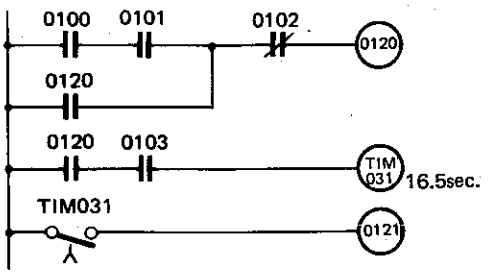
- **Display**



NOTES:

1. When the output relay No. 0120 registered in the No. 0 monitor operates, the LD indicator on the OP display illuminates.
2. When the set time of the timer No. 031 registered in the No. 1 monitor elapses, the AND indicator on the OP display illuminates.

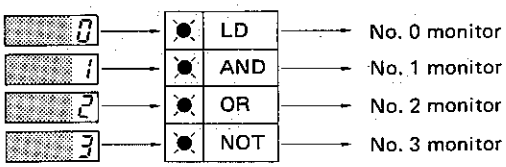
- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	OR	0120
0203	AND-NOT	0102
0204	OUT	0120
0205	LD	0120
0206	AND	0103
0207	TIM	031
0208		165
0209	LD-TIM	031
0210	OUT	0121
0211	END	–

NOTES:

1. During the multi-point monitor operation, the operating states of the relays, etc. registered in the monitor Nos. 0 to 3 displayed on the ADDRESS display will appear in the LD, AND, OR and NOT instruction part of the OP display.



However, the above indicators do not mean that LD, AND, OR and NOT instructions are used during the multi-point monitor operation.

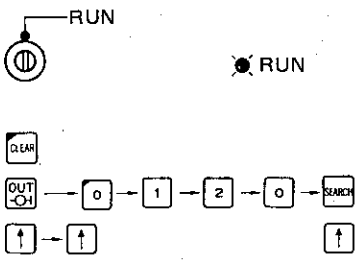
2. Special auxiliary relays such as those for operation result, FAL area, etc. can also be monitored.

6.11 Trace (Continuity) Check Operation

When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.

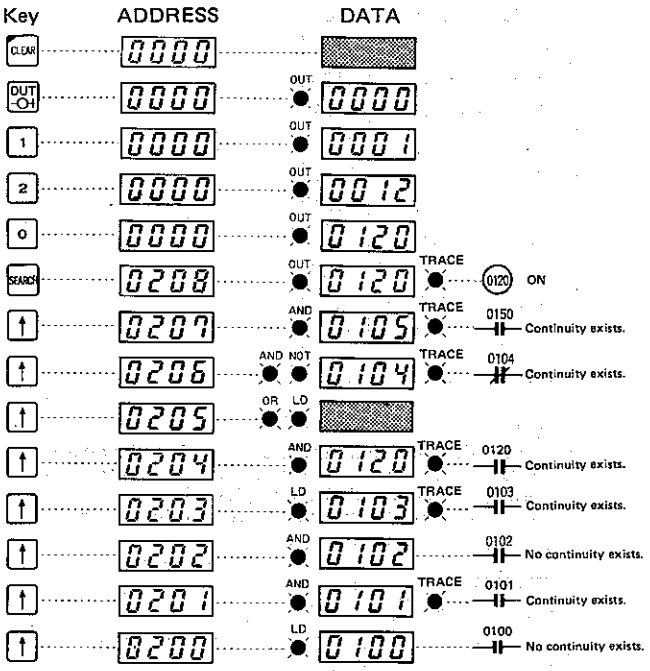
- **Operating procedure**

In the circuit for exercise shown on the right, the procedure to check the operating state of from 0120 to 0100 in the programming sequence is shown below.



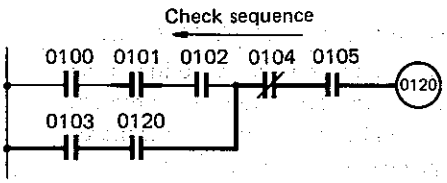
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



NOTES:
1. The above example shows the case where relays 0101, 0103, 0105 and 0150 are in the ON state and relays 0100, 0102 and 0104 are in the OFF state.
2. In the circuit shown on the upper right, is clear that 0120 is caused to turn on by the circuit shown by the bold line.

- **Circuit for exercise and programming examples**



Address	OP	Data
200	LD	0100
201	AND	0101
202	AND	0102
203	LD	0103
204	AND	0120

Address	OP	Data
205	OR-LD	
206	AND-NOT	0104
207	AND	0105
208	OUT	0120
209	END	

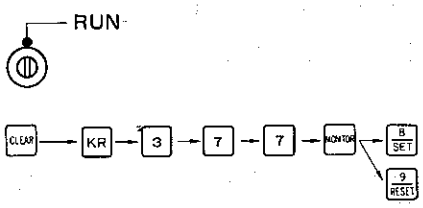
NOTES:
1. The following three methods of trace check are available.
   - Check starting from address 0000
     CLEAR → ↓ ..... ↑
   - Check starting from an OUT instruction.
     Refer to the foregoing operating procedure.
   - Check starting from an END instruction
     CLEAR → FUN → END → SEARCH → ↑ ..... ↓
     In general, an OUT instruction is first searched, and then the continuity of that block is checked according to the programming sequence.
2. The "TRACE" indicator illuminates when continuity exists and goes out when no continuity exists. At the address of AND LD, OR LD, 2nd word of a 2-word instruction, IL, ILC, JMP, JME, SR, MOV, MOV NOT, CMP, +, −, FAL, TR or END instruction, the "TRACE" indicator also goes out.
3. A beep sound is generated upon depression of the ↓ key after the address number has reached "3999." A beep sound is also generated upon depression of the ↑ key when the address number is "0000."

6.12 Forced Set/Reset Operation

This operation is to set or reset by force the operating state of each latching relay, the operating state of each SR bit, or the present value of each timer or counter during the execution of a program. In this forced set/reset operation, the operating state of a relay is caused to be set or reset only the instant the SET or RESET key is depressed, and subsequent circuit operation is the same as originally programmed.

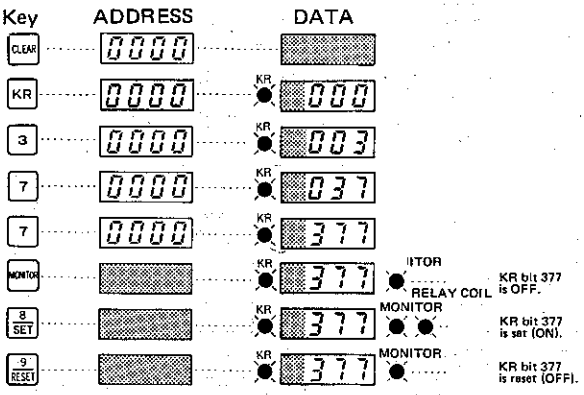
■ SET/RESET OPERATION OF THE LATCHING RELAY

- **Operating procedure**



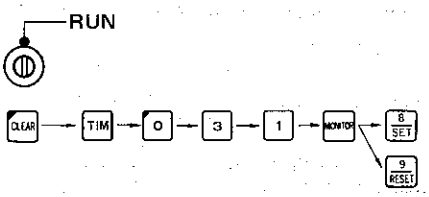
NOTE: The zero key marked 0 may or may not be depressed.

- **Display**

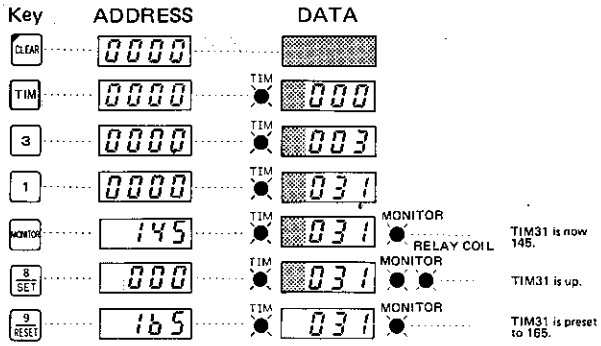


■ SET/RESET OPERATION OF THE PRESENT VALUE OF TIMER AND COUNTER

- **Operating procedure**

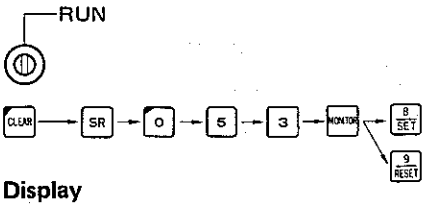


- **Display**

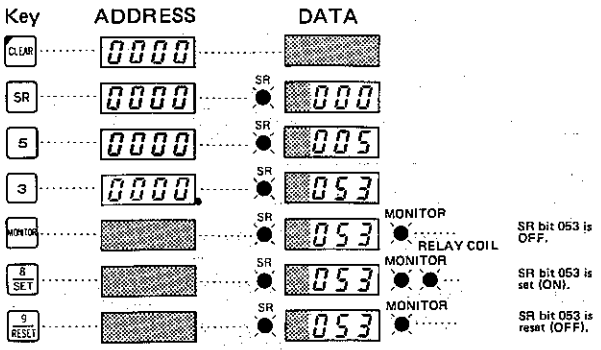


■ SET/RESET OPERATION OF THE SHIFT REGISTER

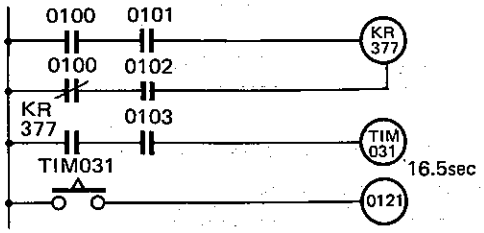
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	LD·NOT	0100
0203	AND	0102
0204	KR	377
0205	LD·KR	377

Address	OP	Data
0206	AND	0103
0207	TIM	031
0208		165
0209	LD·TIM	031
0210	OUT	0121
0211	END	

NOTES:

1. Forced set/reset of the operating state of a latching relay.
   When the SET key is depressed, the operating state of the specified relay number is forcedly turned ON and the "RELAY COIL" indicator illuminates. When the RESET key is depressed, the operating state of the specified relay number is forcedly turned OFF and the "RELAY COIL" indicator goes out.
2. Forced set/reset of the present value of a timer or counter.
   When the SET key is depressed, the present value of the specified timer or counter number is forcedly cleared to zero and the "RELAY COIL" indicator illuminates.
   When the RESET key is depressed, the present value of the specified timer or counter number is forcedly returned to the preset value and the "RELAY COIL" indicator goes out.
3. Forced set/reset of the operating state of an SR bit.
   When the SET key is depressed, the operating state of the specified bit number is forcedly turned ON and the "RELAY COIL" indicator illuminates.
   When the RESET key is depressed, the operating state of the specified bit number is forcedly turned OFF and the "RELAY COIL" indicator goes out.
4. The forced set/reset function is applicable only to latching relays, timers/counters and shift registers.
5. When the SET or RESET key is depressed in any of the following cases, a beep sound is generated to alert the operator. Check for the proper operating procedure.
   1 In the CASSETTE or PROM WRITER mode
   2 During other than the monitoring operation in the RUN mode
   3 When setting other than the address setting and timer or counter data setting is performed in the PROGRAM mode.
   4 While a relay other than latching relay, timer or counter and shift register is being monitored.

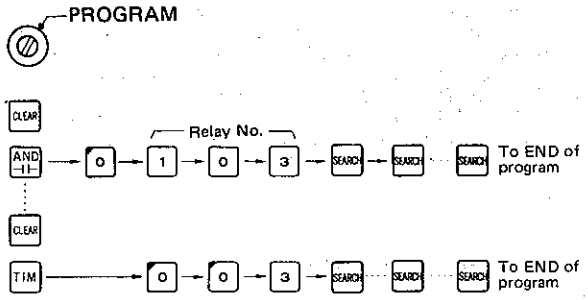
6.13 Instruction Search Operation

When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction or relay number has been written in a program to be searched.

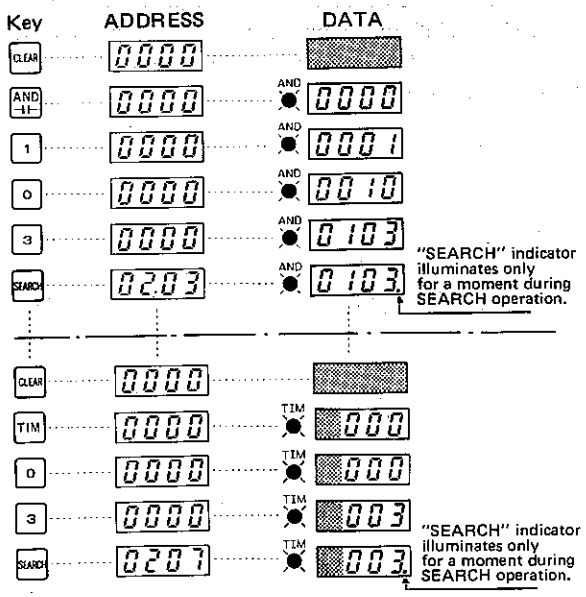
■ SEARCH OPERATION OF INSTRUCTION WORD

- **Operating procedure**

Referring to the circuit for exercise and programming example shown below, an example of searching 0103 —||— and (TIM 003) instructions is explained here.



- **Display**

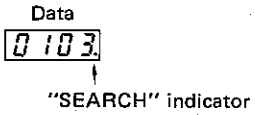


- **Circuit for exercise and programming example**

Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	OR	0120
0203	AND	0103
0204	AND	0104

Address	OP	Data
0205	OUT	0120
0206	LD	0120
0207	TIM	003
0208		35
0209	END	

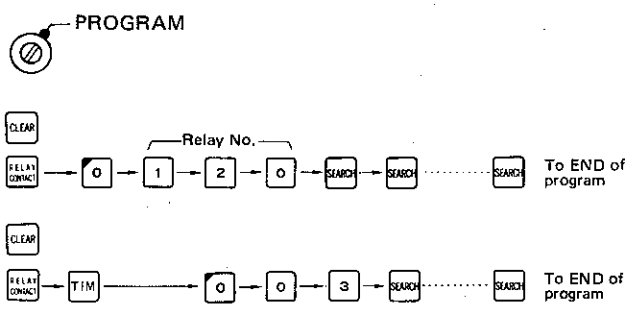
NOTES:
1. When the SEARCH key is depressed after entering an instruction, the first address where the instruction is stored is displayed. Continued depression of the SEARCH key causes all the addresses containing this instruction to be searched until the END instruction is encountered.
2. When the set value of a TIM, CNT instruction is to be searched, the TIM, CNT instruction must be searched before depressing the [↓] key. (The set value cannot be called directly.) The same holds for other 2-word instructions.
3. The "SEARCH" indicator illuminates momentarily while the address of the specified instruction is being searched and goes out upon completion of the search operation.



■ SEARCH OPERATION OF RELAY NUMBER

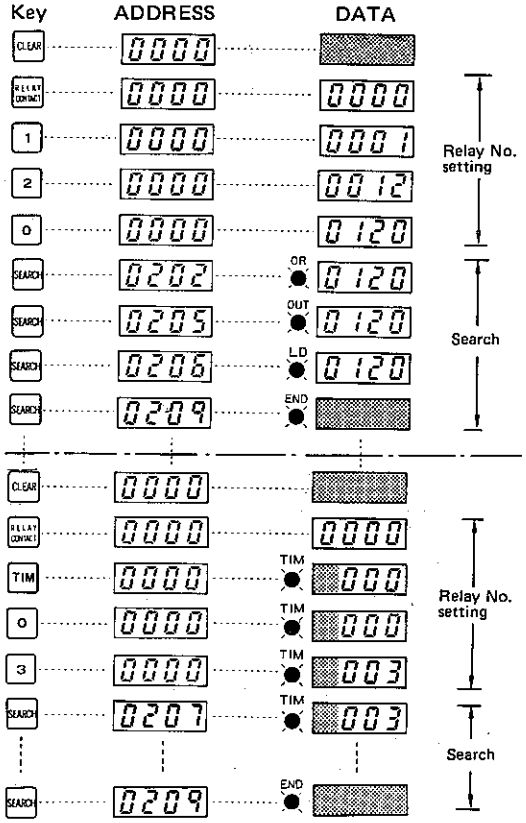
Referring to the circuit for exercise and programming example shown below, an example of searching relay No. 0120 throughout all addresses is explained here.

- **Operating procedure**

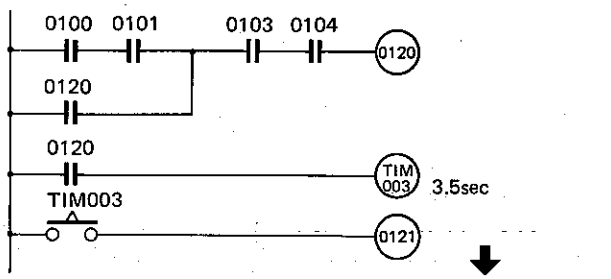


NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	OR	0120
0203	AND	0103
0204	AND	0104
0205	OUT	0120

Address	OP	Data
0206	LD	0120
0207	TIM	003
0208		035
0209	LD-TIM	003
0210	OUT	0121
0211	END	

NOTES:
1. Depress the RELAY CONTACT key, enter the relay number (also depress the OP key in case of a TIM, CNT, SR, KR or TR instruction), and depress the SEARCH key respectively until the last address of a program.
   The CPU stops at each pertinent address where the relay number being searched is located.
   In other words, the relay number search operation is executed from the address being presently displayed to the address when an END instruction is located or to the last address.
   Accordingly, if another relay number is to be searched continuously, depress the CLEAR key once.

2. The second word of a 2-word instruction (TIM, CNT, MOV, CMP, +, −) cannot be searched.
3. The "SEARCH" indicator illuminates momentarily while the address of the specified relay No. is being searched and goes out upon completion of the search operation.

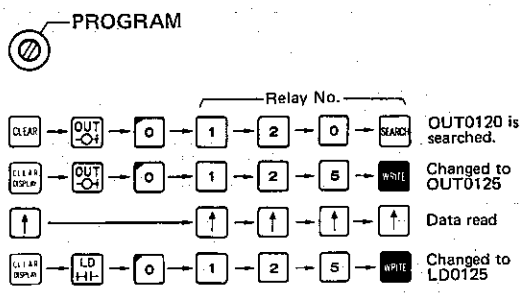
Data

6.14 Contact (Coil) Number Change Operation

This operation is to change the contact (or coil) number in a program due to a circuit modification.

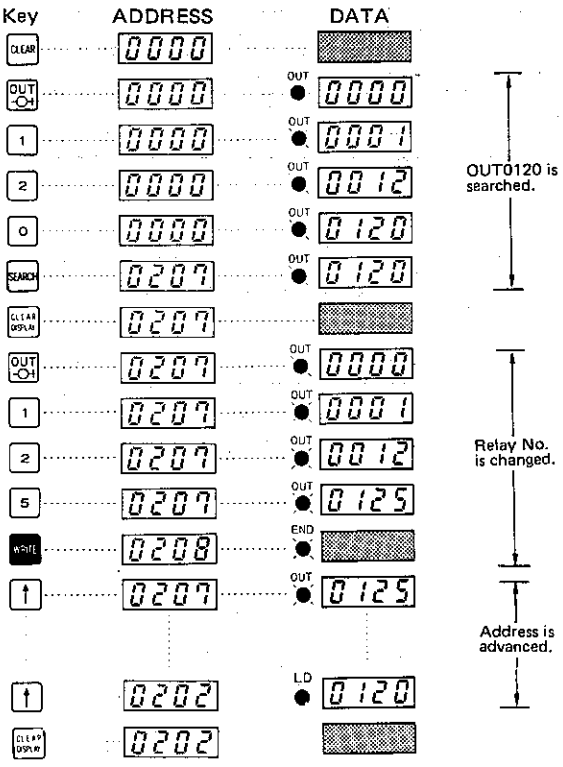
- **Operating procedure**

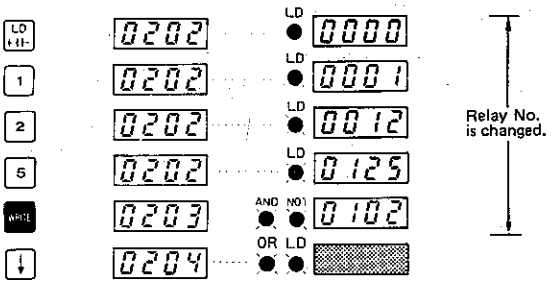
  Referring to the circuit for exercise and programming example shown on the right, an example of changing output relay No. 0120 to 0125 is explained here.



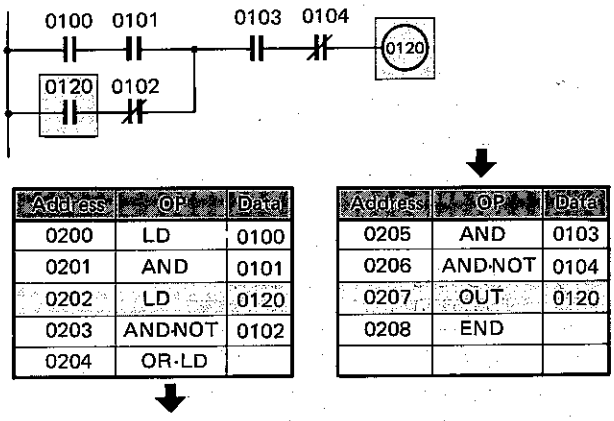
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**





- **Circuit for exercise and programming example**



Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	LD	0120
0203	AND-NOT	0102
0204	OR-LD	

Address	OP	Data
0205	AND	0103
0206	AND-NOT	0104
0207	OUT	0120
0208	END	

NOTES:

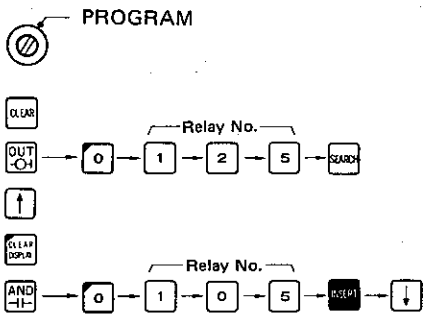
1. After an OUT instruction has been searched, depress the [↑] key continuously to decrement the address number until the address where the contact (coil) number is to be changed. The instruction to be changed at an intended address may be searched directly. However, the same instruction may in some cases be stored in other memory addresses of the same program. Therefore, it is necessary to check instructions before and after the intended address. Since no two OUT instructions with an identical relay number exist in one program, the instruction to be changed can be found easily and quickly by first searching the OUT instruction and then searching before and after the OUT instruction.
2. When changing an instruction, the contact (coil) number setting is also required.
3. When a 2-word instruction is changed to a 1-word instruction, the 2nd word of the 2-word instruction is deleted and all the address numbers after the changed instruction will be decremented by 1.
4. When a 1-word instruction is changed to a 2-word instruction, an address where the 2nd word of the 2-word instruction is to be entered will be automatically secured and all the address numbers after the changed instruction will be incremented by 1. In this case, the "PROGRAM OVER" indicator will illuminate unless the last address has space for 1 word, prohibiting the instruction from being written into memory.
5. When the 1st word of a 2-word instruction is changed, note that the 2nd word of the instruction will be changed to 000.
6. When an OUT, TIM, CNT, SR, KR, MOV, + or − instruction is to be changed to another instruction, also check the circuit related to the instruction.
7. In the above operating procedure, the CLEAR DISPLAY key may be omitted from key entry.
8. After the contact (coil) number has been changed, be sure to perform the Program Check operation ([CLEAR] → [SEARCH]) to confirm that the program is free from any programming error.
9. A beep sound will be generated upon depression of the [↓] after the address number has reached "3999." A beep sound will also be generated upon depression of the [↑] key when the address number is "0000."

6.15 Contact (Coil) Addition Operation

This operation is employed when the contact (or coil) number is to be added due to a circuit modification.

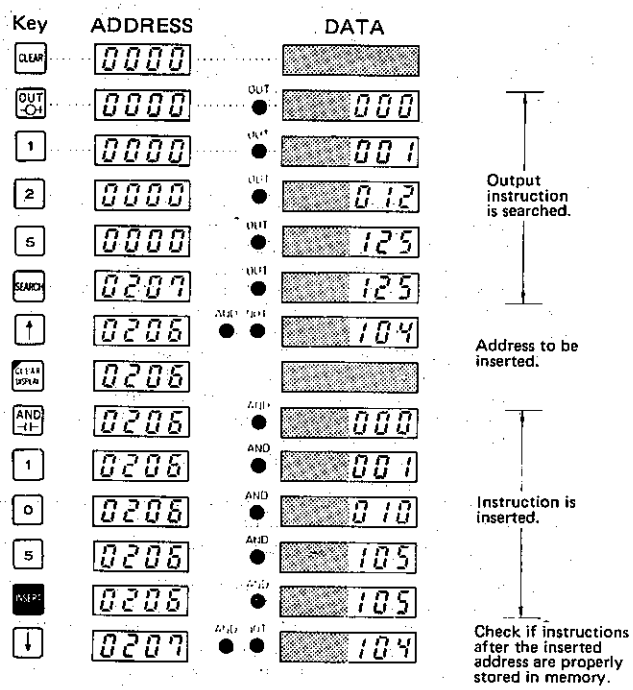
- **Operating procedure**

  In the following the procedure of adding —|0105|— between —|0103|— and —|/0104|— is shown.



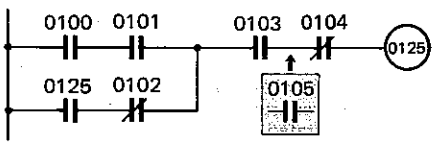
NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



NOTE: The zero key marked [0] may or may not be depressed.

- **Circuit for exercise and programming example**



Before insertion

Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	LD	0125
0203	AND-NOT	0102
0204	OR-LD	
0205	AND	0103
0206	AND-NOT	0104
0207	OUT	0125
0208	END	

After insertion

Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	LD	0125
0203	AND-NOT	0102
0204	OR-LD	
0205	AND	0103
0206	AND	0105
0207	AND-NOT	0104
0208	OUT	0125
0209	END	

NOTES:

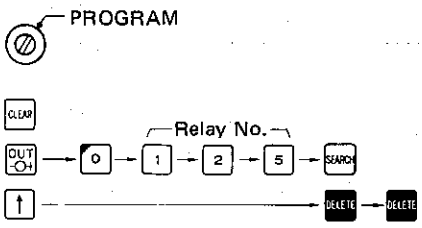
1. Search an OUT instruction, depress the [↑] key repetitively to advance the program up to the address where the instruction is to be inserted. Next, depress the CLEAR DISPLAY key, enter the instruction to be inserted and then depress the INSERT key. The address number after the inserted instruction will automatically be incremented by 1.
2. When a 2-word instruction is inserted, the address where the 2nd word of the 2-word instruction is to be entered will be automatically secured.
3. If a "Program Over" condition occurs as a result of the instruction insertion, the "PROGRAM OVER" indicator illuminates and a beep sound is generated to alert the operator.
4. If an attempt is made to insert an instruction into the address where the 2nd word of a 2-word instruction has been set, a beep sound is generated to signal the operator that the instruction cannot be inserted.
5. In other than the PROGRAM mode, no instruction can be inserted and a beep sound is generated to alert the operator.
6. After the instruction to be inserted has been entered, depression of the INSERT key two or more times in succession will be ignored and no instruction can be entered. In this case, a beep sound will also be generated to alert the operator.
7. After the insertion of the instruction, confirm instructions before and after the inserted address.
8. After the contact (coil) number has been inserted, be sure to perform the Program Check operation ([CLEAR] → [AND]) to confirm that the program is free from any programming error.
9. When the user memory is not equipped fully with 4K words of RAMs, no "PROGRAM OVER" check can be performed.

6.16 Contact (Coil) Deletion Operation

This operation is to delete contact (or coil) number(s) from a program due to a circuit modification.

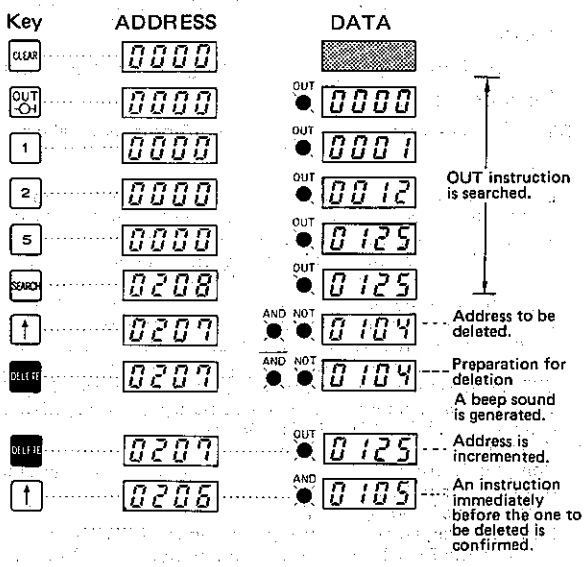
- **Operating procedure**

  Referring to the circuit for exercise shown below, an example of deleting —|/0104|— is explained.

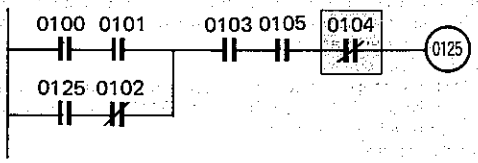


NOTE: The zero key marked [0] may or may not be depressed.

- **Display**



- **Circuit for exercise and programming example**



Before deletion

Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	LD	0125
0203	AND-NOT	0102
0204	OR-LD	

Address	OP	Data
0205	AND	0103
0206	AND	0105
0207	AND-NOT	0104
0208	OUT	0125
0209	END	

After deletion

Address	OP	Data
0200	LD	0100
0201	AND	0101
0202	LD	0125
0203	AND-NOT	0102
0204	OR-LD	

Address	OP	Data
0205	AND	0103
0206	AND	0105
0207	OUT	0125
0208	END	
0209		

NOTES:

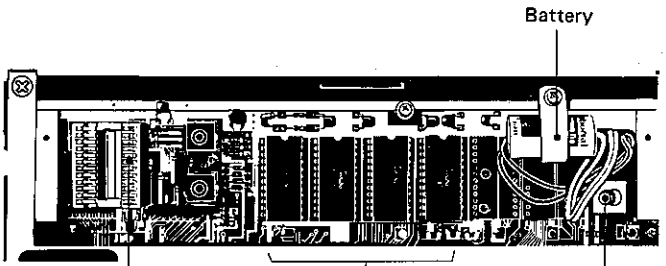
1. Search an OUT instruction, depress the ↑ key to advance the program up to the address where the instruction to be deleted is located, and depress the DELETE key twice in succession. All the address numbers after the deleted instruction will automatically be decremented by 1.
   The reason for depressing the DELETE key twice is to prevent an instruction from being deleted accidentally due to an erroneous key operation. The first depression of the key causes a beep sound to be generated to signal the preparation for an instruction deletion. The second and each subsequent depression of the key cause instructions to be deleted one by one.
2. When a 2-word instruction (TIM, CNT, MOV, +, or −) is deleted, the address where the address of the 2nd word is located will also be deleted automatically.
3. Only the 2nd word of a 2-word instruction (TIM, CNT, MOV, +, −) cannot be deleted. A beep sound generated if an attempt is made to do so.
4. After the instruction has been deleted, confirm instructions before and after the deleted address.
5. After the deletion of the instruction, be sure to execute the Program Check operation (CLEAR → SEARCH). Particularly, the program check is mandatory when input, output or clock contact of such an instruction as TIM, CNT, SR or KR is deleted.
6. When the DELETE key is depressed in the CASSETTE, RUN or PROM WRITER mode, a beep sound is generated to alert the operator.

7. EPROM Chip and Cassette Tape Handling

7.1 Basic Functions

Items of operation	Description
EPROM write	This operation is to transfer the contents of any of the memory Nos. 0 ~ 3 in the user memory (RAM/ROM) program area to the EPROM chip mounted on the PROM socket.
EPROM read	This operation is to transfer the contents of the EPROM chip (mounted on the PROM socket) to any of the memories 0 ~ 3 in the user program (RAM) memory area.
EPROM verify	This operation is to verify the contents of the EPROM chip (mounted on the PROM socket) against the contents of any of the memory Nos. 0 ~ 3 in the user program (RAM) memory area.
Tape write	This operation is to record the contents of the user program (RAM/ROM) on a cassette tape.
Tape read	This operation is to transfer the program data recorded on the cassette tape into the user program (RAM).
Tape verify	This operation is to verify the contents of the user program (RAM/ROM) against the programmed data recorded on a cassette tape.

7.2 RAM and EPROM Chip Handling



User program memory
Memory No. 0 : Address 0000 ~ 1023
Memory No. 1 : Address 1024 ~ 2047
Memory No. 2 : Address 2048 ~ 3071
Memory No. 3 : Address 3072 ~ 3999

■ TO USE RAM MEMORY

1. Set the RAM/ROM selector switch to the "RAM" position.
2. Mount RAM chip(s) in the user program memory area (Memory No. 0 ~ 3).

NOTE: Applicable memory element: 5516 or its equivalent

CAUTION:
Do not turn the RAM/ROM selector switch to the "ROM" position while the RAM memory is in use, or the program may be destroyed.

■ TO USE ROM MEMORY

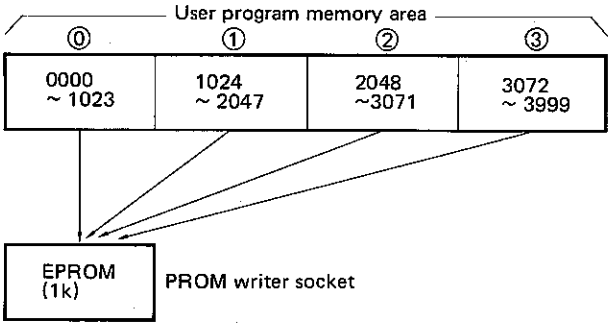
1. Set the RAM/ROM selector switch to the "ROM" position.
2. Mount ROM chips in the user program memory area (Memory No. 0 ~ 3).

NOTE: Applicable memory element: 2716 or its equivalent

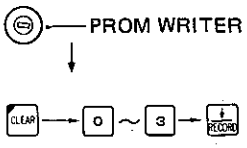
NOTES:
1. Do not remove or insert any user program memory chip (RAM/ROM) while power is being applied to the SYSMAC-M1R. Otherwise, the memory chip may be destroyed.
2. Completely erase the EPROM and then write data into the EPROM. The contents of the EPROM are erased by irradiating ultraviolet rays on the EPROM surface through the erase window. The EPROM cannot be erased completely if the irradiation by ultraviolet rays is insufficient. Therefore, be sure to observe the specified erase time. Whether or not the EPROM has been erased completely can be confirmed by the EPROM Verify operation. (Refer to paragraph 7.10, Errors in PROM WRITER or CASSETTE Mode.)
3. Erase time
   Completely erase the EPROM according to the specifications of the eraser to be used.
4. Frequency of re-programming
   Limit the frequency of re-programming the EPROM to 7 times. If the EPROM is re-programmed more than 7 times, the EPROM may malfunction.
5. Program protection
   To sustain the reliability of the EPROM, place the EPROM in a protective case or wrap it in aluminum for if it is not to be used for an extended period.
6. Handling EPROM
   The EPROM is susceptible to static electricity being carried in the human body. When handling the EPROM, avoid touching its pins as much as possible.
7. Removal of EPROM
   The EPROM can be inserted or removed while power is being applied to the SYSMAC-M1R. However, never remove the EPROM chip during the EPROM write, read, or verify operation.
8. After the program debugging, be sure to attach a light-shielding seal to the erase window in order to maintain the reliability of the EPROM chip.

7.3 EPROM Write Operation

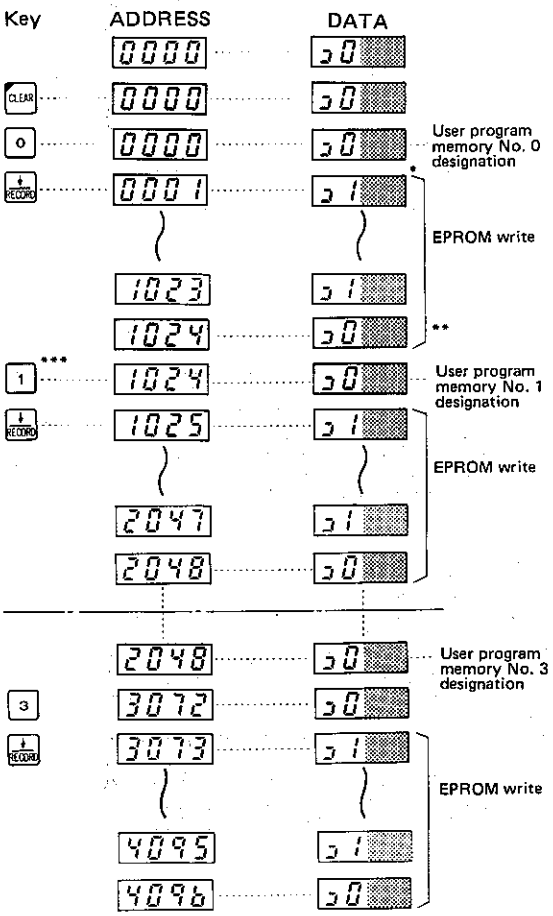
This operation is to transfer the contents of any of the memory Nos. 0 ~ 3 in the user program (RAM/ROM) memory area to the EPROM chip mounted on the PROM writer socket.



- **Operating procedure**



- **Display**



* 01 on the DATA display indicates that the EPROM Write operation is being executed.

** 00 on the DATA display indicates that the EPROM Write operation has been completed. The next address for EPROM write is indicated on the ADDRESS display.

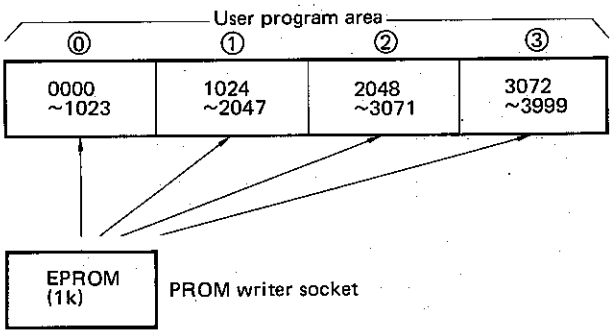
*** For example, to perform the EPROM Write operation from memory No. 1, depress the CLEAR key, specify memory No. 1 by depressing numeric key and then depress the RECORD key.

NOTES:

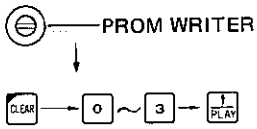
1. One of memory Nos. 0 ~ 3 must be specified. However, when the EPROM Write operation is to be performed successively from the memory No. 0, this memory number designation is not required.
2. Upon depression of the RECORD key, EPROM erase check is performed, and then the EPROM Write operation will start.
3. During the EPROM Write operation, if the power is turned off, or the EPROM chip is removed, the EPROM Write will be interrupted. In such a case, retry the EPROM write operation from the beginning after erasing the EPROM chip, or use other EPROM area.
4. During the EPROM Write operation, no PROGRAM key input will be accepted.
5. When any error occurs during the EPROM Write operation, the buzzer issues intermittent beep sounds to alert the operator.
6. After the EPROM Write operation, be sure to perform the EPROM Verify operation to check if the data have been written properly into the EPROM.
7. To stop the EPROM Write operation under execution, either depress the CLEAR key or operate the mode selector switch (to other than the PROM WRITER position).

7.4 EPROM Read Operation

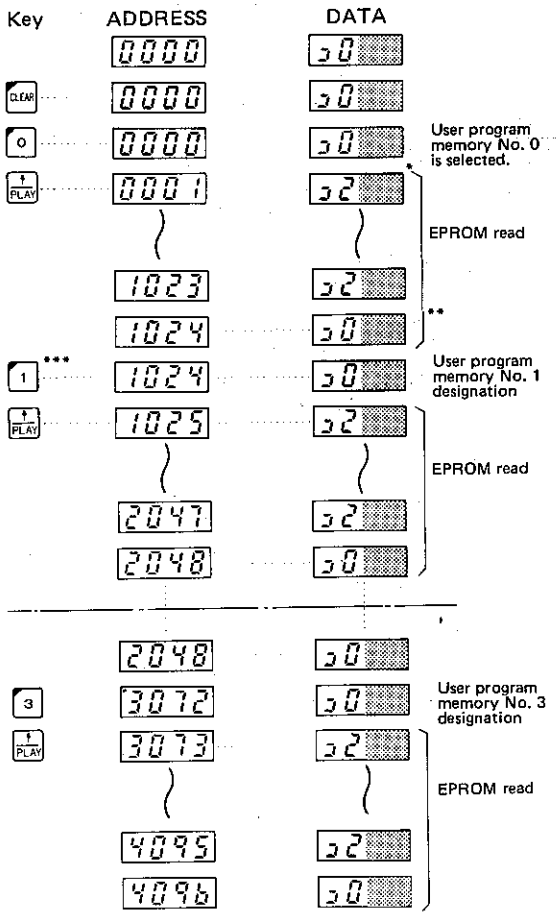
This operation is to transfer the contents of the EPROM chip (mounted on the PROM writer socket) to any of the memory Nos. 0 ~ 3 in the user program (RAM) memory area.



- **Operating procedure**



- **Display**

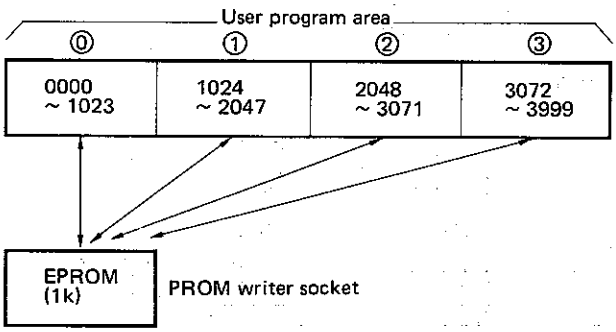


* 32 on the DATA display indicates that the EPROM Read operation is being executed.
** 30 on the DATA display indicates that the EPROM Read operation has been completed and the next address for EPROM read is indicated on the ADDRESS display.
*** For example, to transfer the EPROM chip data into memory No. 1, depress the CLEAR key, specify memory No. 1 by depressing numeric key 1 and then depress the PLAY key.

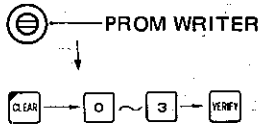
NOTES:
1. One of memory Nos. 0 ~ 3 must be specified. However, when the EPROM Read operation is to be performed successively from the memory No. 0, this memory number designation is not required.
2. During the EPROM Read operation, if the power is turned off or the EPROM chip is removed, the EPROM read will be interrupted. In such a case, retry the operation from the beginning.
3. When an error occurs during the EPROM Read operation, the buzzer issues intermittent beep sounds to alert the operator.
4. Be sure to perform the EPROM Verify operation to check if the data have been read properly by the RAM.
5. Upon completion of the EPROM Read operation, the specified memory No. will be indicated on the MEMORY No. display.
6. To stop the EPROM Read operation under execution, either depress the CLEAR key or operate the mode selector switch (to other than PROM WRITER).

7.5 EPROM Verify Operation

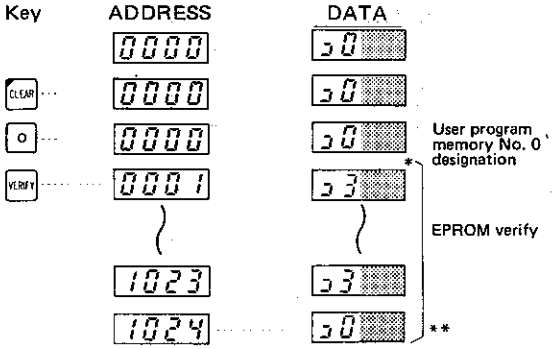
This operation is to verify the contents of the EPROM chip (mounted on the PROM writer socket) against the contents of any of the memory Nos. 0 ~ 3 in the user program (RAM) area.

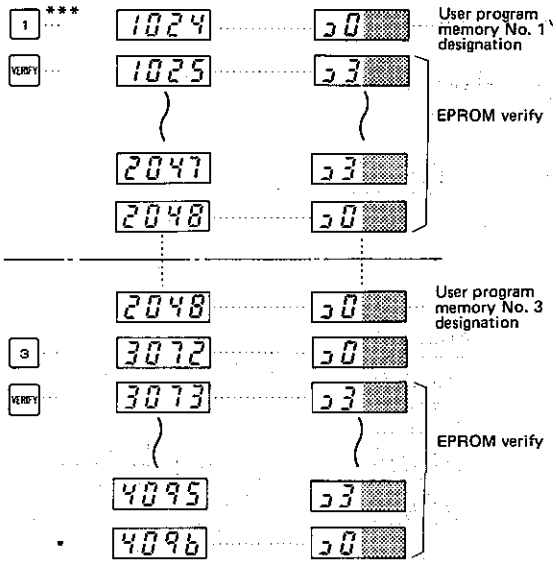


- **Operating procedure**



- **Display**



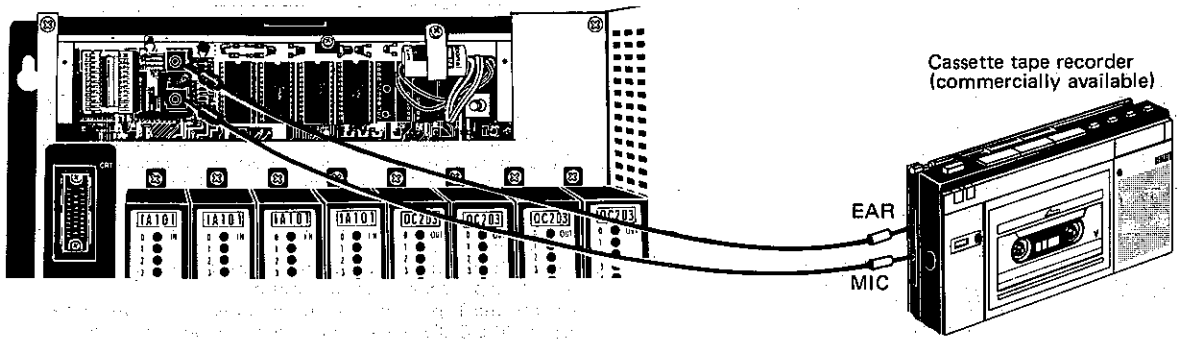


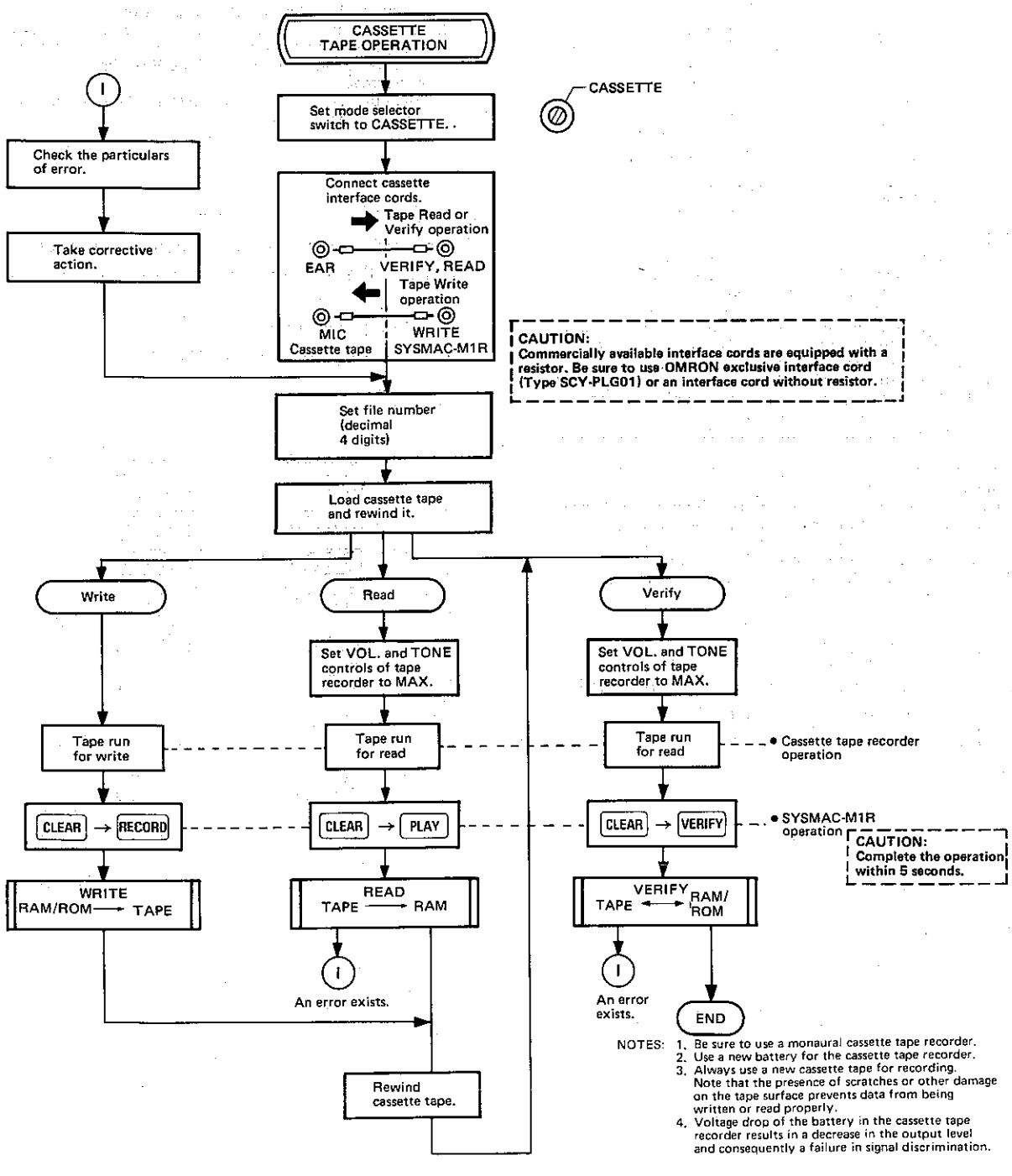
* 33 on the DATA display indicates that the EPROM Verify operation is being executed.
** 30 on the DATA display indicates that EPROM Verify operation has been completed and the next address for EPROM verify is indicated on the ADDRESS display.
*** For example, to perform EPROM Verify operation between the EPROM chip and memory No. 1, depress the CLEAR key, specify memory No. 1 by depressing numeric key 1, and then depress the VERIFY key.

NOTES:
1. One of memory Nos. 0 ~ 3 must be specified. However, when the EPROM Verify operation is to be performed successively from the memory No. 0, this memory number designation is not required.
2. During the EPROM Verify operation, if the power is turned off, or the EPROM chip is removed, the EPROM Verify operation will be interrupted. In such a case, retry the operation from the beginning.
3. When an error occurs during EPROM Verify operation, the buzzer issues intermittent beep sounds to alert the operator.
4. To stop the EPROM Verify operation under execution, either depress the CLEAR key or operate the mode selector switch (to other than the PROM WRITER position).

7.6 Cassette Tape Handling

As a method of keeping user programs in storage, data may be recorded on a cassette tape by using a commercially available cassette tape recorder.
In the following, a general operational flowchart is shown.





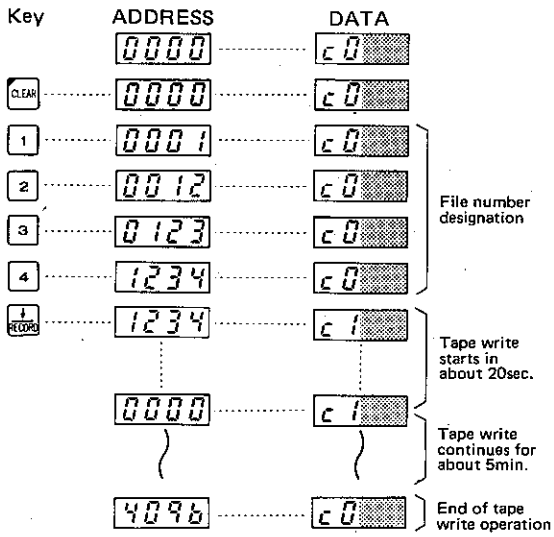
NOTES:
1. Be sure to use a monaural cassette tape recorder.
2. Use a new battery for the cassette tape recorder.
3. Always use a new cassette tape for recording. Note that the presence of scratches or other damage on the tape surface prevents data from being written or read properly.
4. Voltage drop of the battery in the cassette tape recorder results in a decrease in the output level and consequently a failure in signal discrimination.

7.7 Tape Write Operation

This operation is to record the contents of the user program (RAM/ROM) on a cassette tape.

- **Operating procedure**
  Refer to 7.6, Cassette Tape Handling.

- **Display**



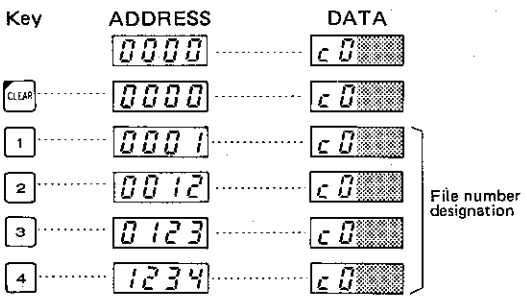
NOTES:
1. Upon completion of the Tape Write operation, be sure to perform the Tape Verify operation to confirm that the data have been recorded on the tape properly.
2. Error detection cannot be performed during the Tape Write operation. Even if the tape does not run, data will be transferred unilaterally from the RAM/ROM. So, be sure to confirm that the tape is running smoothly.
3. If the power is turned off or the cassette is ejected during the Tape Write operation, the tape write will be interrupted. Retry the tape write operation from the beginning.
4. During the Tape Write operation, no PROGRAM key input will be accepted.
5. For the Tape Write operation, use the WRITE → MIC jack to connect one of the cassette tape interface cords. For subsequent verify operation, use VERIFY READ ← EAR jack.
6. To stop the Tape Write operation under execution, either depress the CLEAR key or by operate the mode selector switch (to other than the CASSETTE position).
7. Any 4-digit file number may be designated by the user.

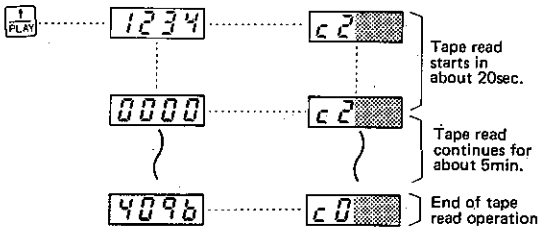
7.8 Tape Read Operation

This operation is to transfer the program data recorded on the cassette tape into user program (RAM).

- **Operating procedure**
  Refer to 7.6, Cassette Tape Handling.

- **Display**





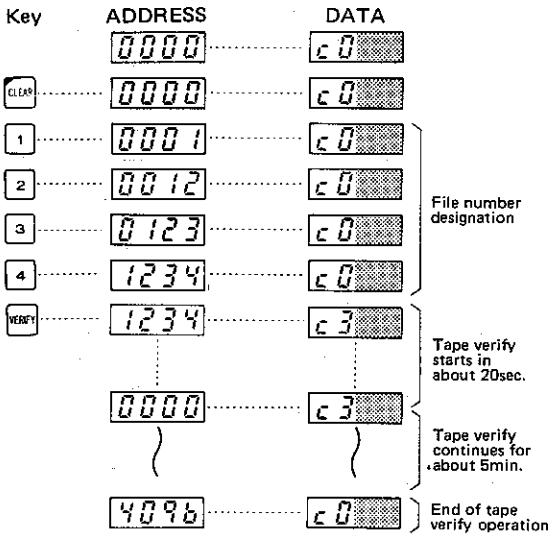
NOTES:
1. Upon completion of the Tape Read operation, be sure to perform the Tape Verify operation to confirm that the data have been transferred properly from the tape to the RAM.
2. If the power is turned off or the cassette is ejected during the Tape Read operation, the tape read will be interrupted. Retry the tape read operation from the beginning.
3. During the Tape Read operation, no PROGRAM key input will be accepted.
4. Be sure to set the volume control and tone control of the cassette tape recorder to maximum.
5. To stop the Tape Read operation under execution, either depress the CLEAR key or operate the mode selector switch (to other than the CASSETTE position).
6. If the file number does not coincide with the file number recorded in the Tape Write operation, this condition is regarded as an error and no Tape Read operation will be performed.
7. File number entry must be performed before running the tape for read.

7.9 Tape Verify Operation

This operation is to verify the contents of user program (RAM/ROM) against the programmed data recorded on a cassette tape.

- **Operating procedure**
  Refer to 7.6, Cassette Tape Handling.

- **Display**



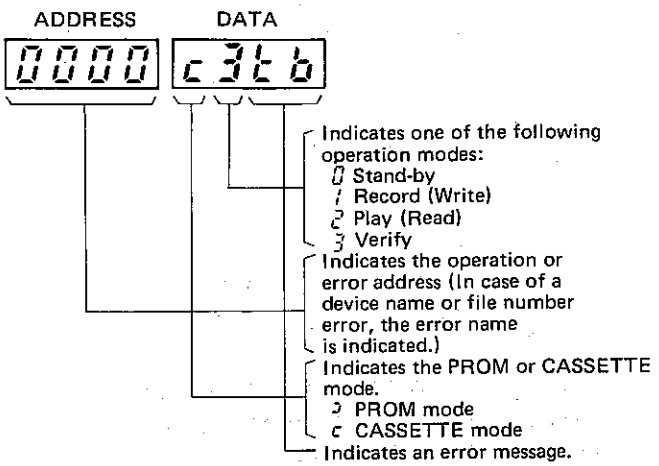
NOTES:
1. If the power is turned off or the cassette tape is ejected during the Tape Verify operation, the tape read will be interrupted. Retry the Tape Verify operation from the beginning.
2. During the Tape Verify operation, no PROGRAM key input will be accepted.
3. Be sure to set the volume control and tone control of the cassette tape recorder to maximum.
4. To stop the Tape Verify operation under execution, either depress the CLEAR key or operate the mode selector switch (to other than the CASSETTE position).

5. If the number does not coincide with the file number recorded in the Tape write operation, the condition is regarded as an error and no Tape Verify operation will be performed.
6. File number entry must be performed before running the tape for verify.

7.10 Errors in PROM WRITER or CASSETTE Mode

In the PROM WRITER or CASSETTE mode, the following indications may appear on the ADDRESS and DATA displays, respectively.

- **Display**



■ DESCRIPTION OF ERROR MESSAGE

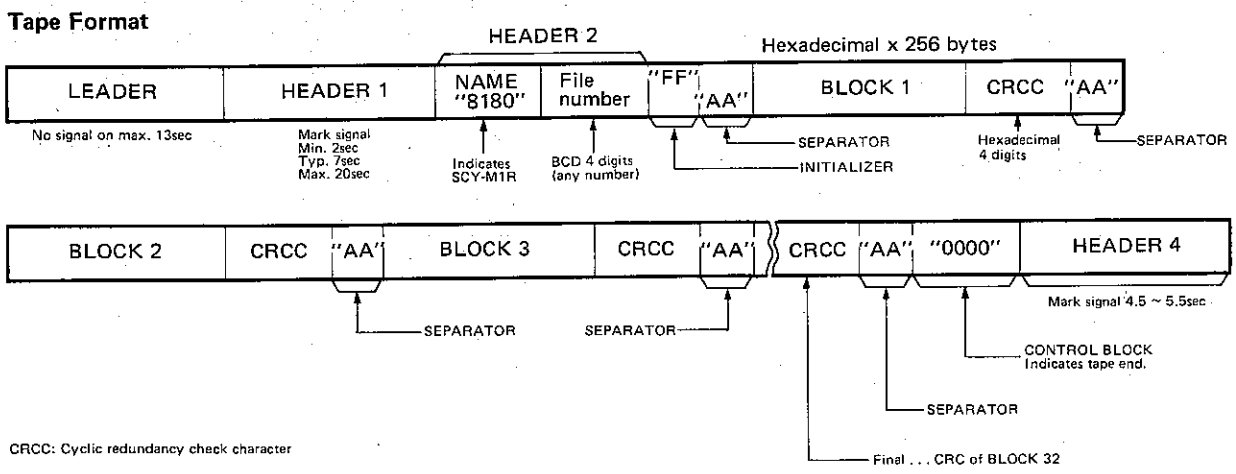
- **PROM Mode**

Operation	Error message	Description of message
EPROM write	1tb	Verify error (as a result of verify check for each written word)
	1t7	Erase check error (as a result of the EPROM erasure check before EPROM write)
EPROM verify	3tb	Verify error (as a result of EPROM Verify operation)

- **CASSETTE Mode**

Operation	Error message	Description of message
Tape read	2t1	Framing error (2 stop bits do not exist for one start bit)
	2t2	CRC check error (as a result of CRC check of one block (128 words or 256 bytes) of data)
	2t3	Time out error (HEADER 2 (device or file number) is not output within 35 sec after the start of the tape read operation.)
	2t4	Format error (Initializer or separator code is abnormal.)
	2t7	Device name error (The device name is other than the code "8180" of the SYSMAC-M1R in the tape read operation.)
	2t8	File number error (The recorded file number does not coincide with the file number entered by key operation.)
Tape verify	3t1	Framing error (2 stop bits do not exist for one start bit.)
	3t2	CRC check error (as a result of the CRC check of one block (128 words or 256 bytes) of data.)
	3t3	Time out error (HEADER 2 (device or file number) is not output within 35sec after the start of tape verify operation.)
	3t4	Format error (Initializer or separator code is abnormal.)
	3tb	Verify error (Data recorded on the tape does not coincide with that stored in the user program memory.)
	3t7	Device name error (The device name is other than the code "8180" of the SYSMAC-M1R in the tape verify operation.)
	3t8	File number error (The recorded file number does not coincide with the file number entered by key operation.)

- **Tape Format**



NOTE:
For information on the Graphic programming console (CRT) Model SCY-CRT10-81E(-82E), please refer to the OMRON Graphic Programming Console Model SYSMAC-CRT10 User's Manual (Cat. No. W50-E1) published under separate cover.

8. Installation and Wiring

The SYSMAC-M1R is a highly reliable programmable controller which is resistant to adverse environmental conditions. However, in order to permit the programmable controller to fully exhibit its functions, as well as to enhance its reliability, care must be exercised on the following points when installing the programmable controller.

8.1 Mounting Locations and Environmental Conditions

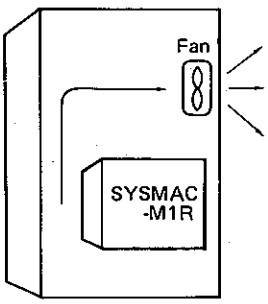
When installing the SYSMAC-M1R programmable controller, avoid the following locations.

- Location where the ambient temperature is beyond the range of 0 to 50°C.
- Location where temperature changes abruptly, thus resulting in condensation.
- Location where relative humidity exceeds the range of 30 to 90%.
- Location subject to corrosive gas or flammable gas.
- Location subject to excessive dust, salt, or iron particles.
- Location subject to vibration or shock.
- Location subject to direct sunlight.

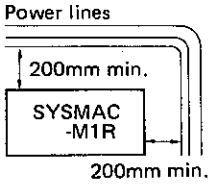
8.2 Mounting Positions within Control Panels

When mounting the SYSMAC-M1R in a control panel, take into consideration the operability, maintenability and environmental resistance of the programmable controller.

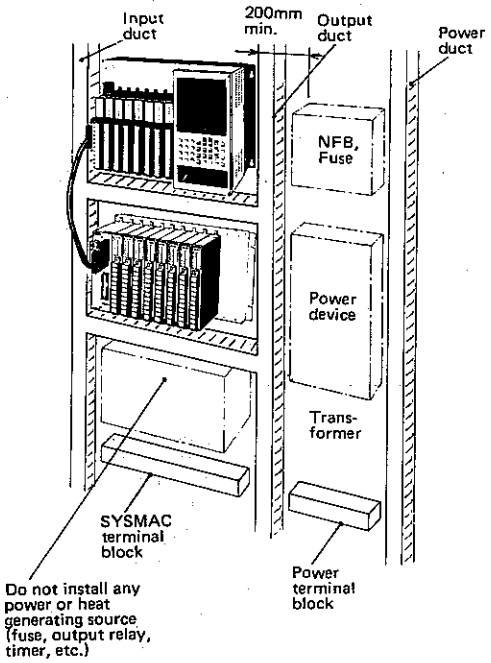
1. To permit the use of the SYSMAC-M1R within the ambient operating temperature range, pay attention to the following points.
   a. Provide the programmable controller with adequate space for ventilation.
   b. Avoid mounting the controller directly above any heat generating sources (heater, transformer, resistor of high capacity).
   c. Install a fan for forced ventilation if the ambient temperature exceeds 50°C.



2. Avoid mounting the SYSMAC-M1R in a panel in which high-tension equipment is installed.
3. Provide a distance of more than 200mm between the high-tension or power lines and the SYSMAC-M1R.



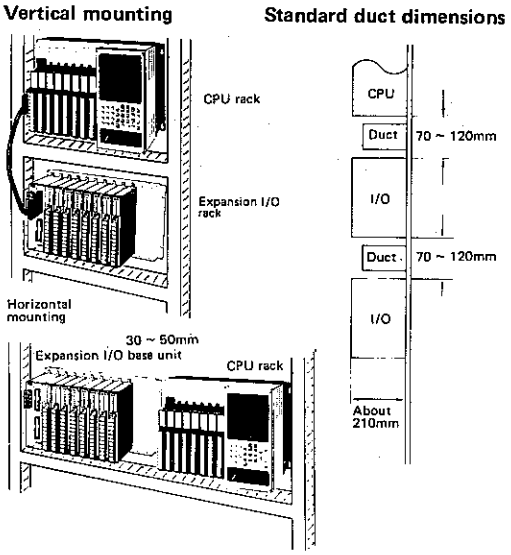
4. Mount the SYSMAC-M1R as far away as possible from high-tension equipment or power devices for the sake of safety in maintenance and operation.



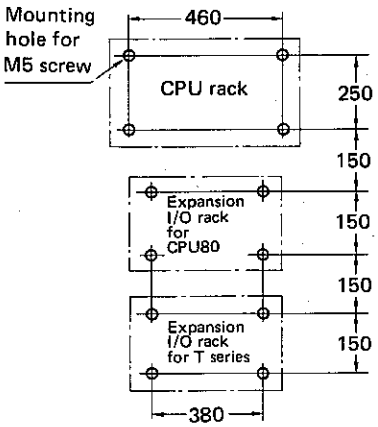
5. Mounting the SYSMAC-M1R at a height 1,000 to 1,600mm above the installed surface of the control panel will facilitate the operation of the programmable controller.

8.3 How to Install within Control Panels

1. When mounting the SYSMAC-M1R programmable controller within a control panel, the CPU rack is normally mounted above the expansion I/O rack with each unit secured to the mounting panel within the control panel. When mounting an expansion I/O rack at the side of the CPU rack, the expansion I/O rack must be located on the left side of the CPU rack. A mounting space of 70 ~ 120mm is required between the CPU rack and an expansion I/O rack or between any two expansion I/O racks for vertical mounting, with consideration given to the space required for wiring ducts and the method of wiring.

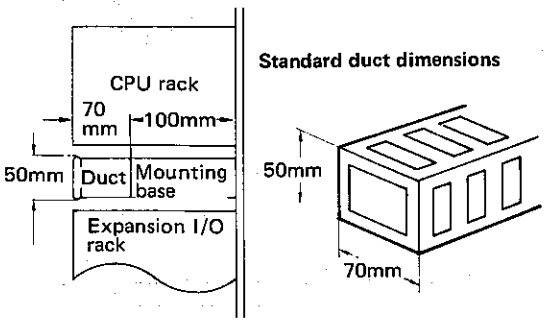


2. Mounting dimensions



3. Wiring ducts

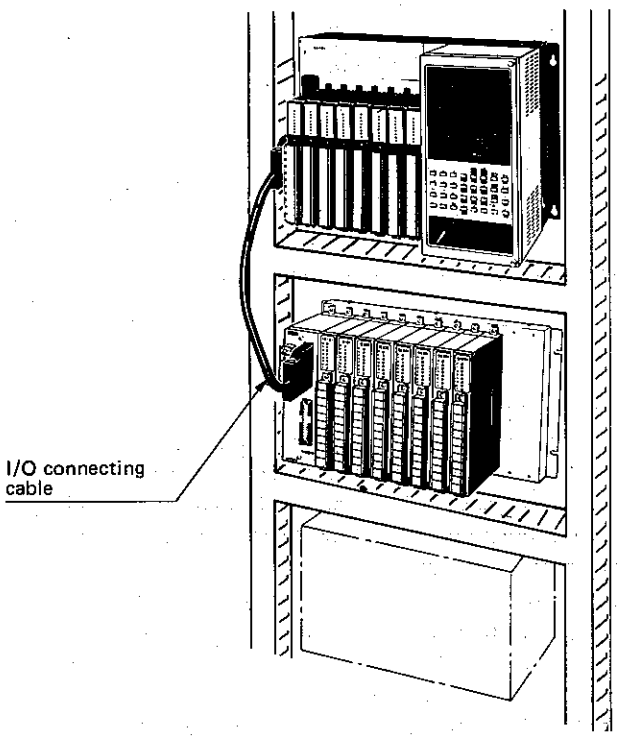
Use of wiring ducts is recommended for the external wiring of I/O units. Provide each wiring duct with a mounting base to facilitate the wiring from each I/O unit so that the height of the wiring duct becomes nearly the same as that of the expansion I/O rack.



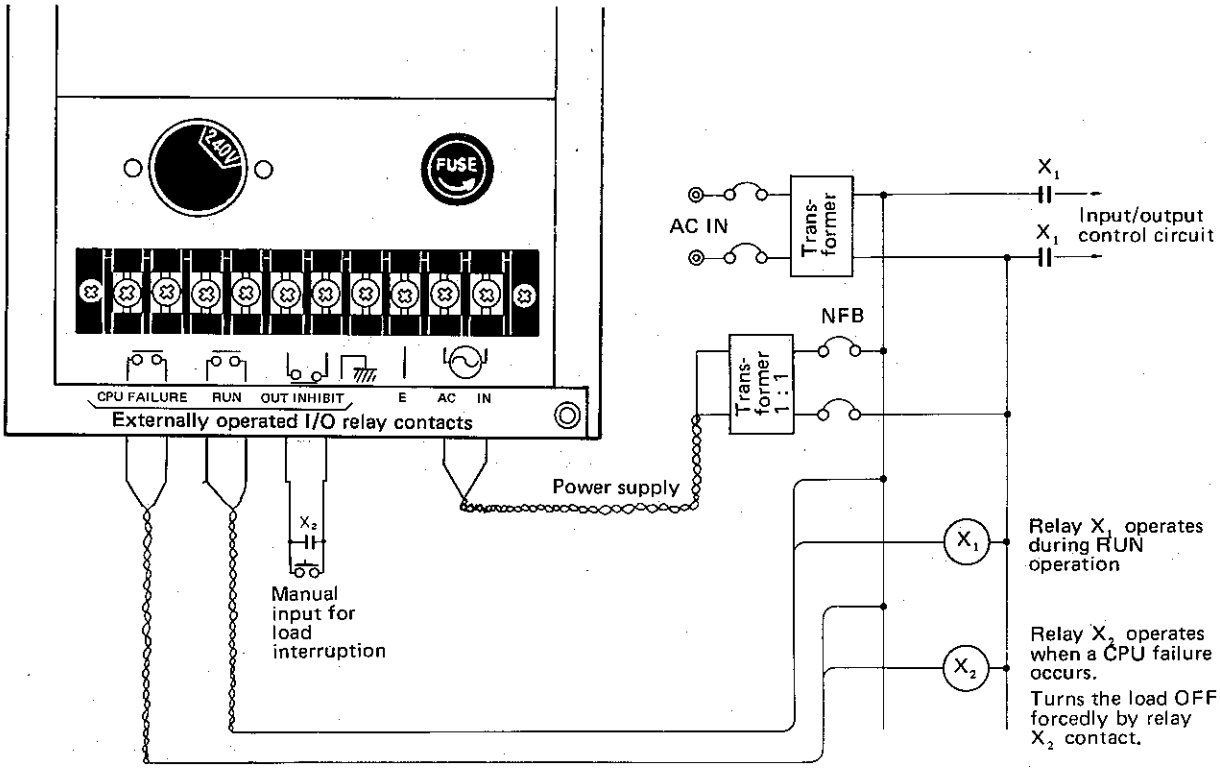
8.4 Processing of Wiring within Control Panels

1. Pay attention to the following points for wiring within a control panel.

- Avoid accommodating the power supply cable (5V) for expansion I/O rack and the I/O connecting cable in the same duct for other wiring.
- Use twisted pair wires of 2mm^2 min. as the power supply cable (DC 5V, 0V) for expansion I/O rack and keep them separate from high-tension or power lines and input/output lines.
- Connect the ground wire to the terminal G on the operating panel of the CPU rack. Use a wire of more than 2mm^2 for grounding.
- Complete the wiring so that the I/O lines do not touch the CPU rack.
- Complete the wiring so as to facilitate the mounting and removal of I/O units.
- Complete the I/O wiring so that the I/O operation indicators on each I/O unit is easily visible.



2. About wiring and power supply

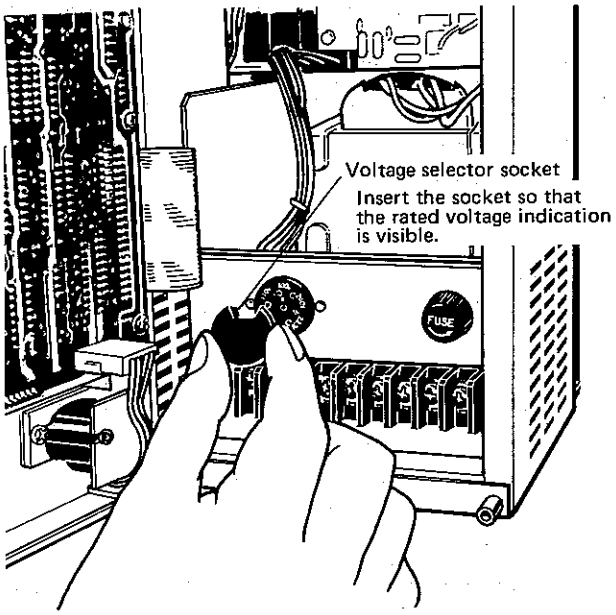


NOTE: * Refer to Section 8.7 for the hints on use of the externally operated I/O relay contact.

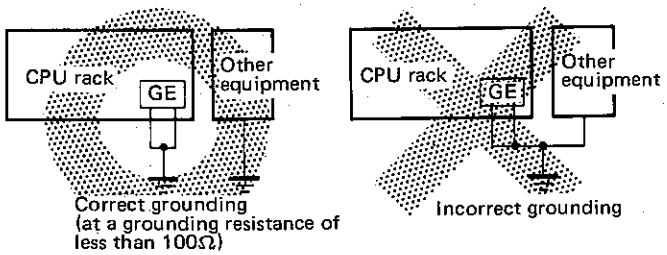
- Power supply capacity
  The power consumption of the SYSMAC-M1R is less than 110VA. However, upon power application, inrush current of about 5 times the steady-state current will flow through the programmable controller. Take this point into account.
- Before power application, be sure to set desired supply voltage using the voltage selector socket. (This socket is factory-set to AC 240V prior to shipment.) Also confirm that the power switch located at the lower right side of the CPU is in the "ON" position. (This switch is factory-set to the ON position prior to shipment.)
- As the power supply line of the SYSMAC-M1R, employ a wire of 2mm^2 min. so as to prevent voltage drop. (Use of twisted pair wires is recommended.)
- For general noise on the power supply line, the noise suppressing circuit in the SYSMAC-M1R is sufficient. However, supplying power through a transformer having a transformer voltage ratio of 1:1 will help reduce equipment-to-ground noise to a great extent and installation of such a transformer is recommended.
  Terminal G of the I/O unit is a ground terminal used for prevention of electric shock. Use an exclusive ground wire (having a conductor cross-sectional area of 2mm^2 min.) for grounding at a grounding resistance of less than 100Ω.

Terminal E is a noise filter neutral terminal and the grounding is not basically required. In case of a large noise which may cause an erroneous operation, E and G are short-circuited for exclusive grounding (at a grounding resistance of less than 100Ω).
Note that common use of the grounding line with other equipment or connecting to the beam of the building may adversely affect the system.
Keep the length of the ground wire within 20m. Care must be taken to the grounding resistance as it varies depending on the nature of ground, water content, season and the time elapsed after the underground laying of the ground wire.

- Supply voltage setting method



- Grounding with other equipment



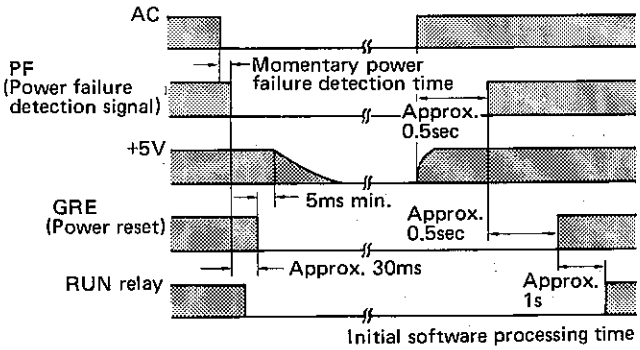
8.5 Operation at Power Failure

1. As the power supply of the SYSMAC-M1R, supply power within +10%, −15% of the supply voltage.
2. The power sequence circuit is incorporated in the power supply unit of the SYSMAC-M1R to prevent the programmable controller from malfunctioning due to a momentary power failure or a decrease in the supply voltage.
   a. Supply voltage drop
      If the supply voltage drops below its 85%, the operation of the SYSMAC-M1R stops, causing external output relays to turn off.
   b. Momentary power failure

0 ~	1 ~	2 cycle
Ignores	Indefinite	Detects power failure

   1. The SYSMAC-M1R ignores a momentary power failure not exceeding 1 cycle of power frequency.
   2. The SYSMAC-M1R either ignores or detects a momentary power failure exceeding 1 cycle but not exceeding 2 cycles of power frequency.
3. Should a momentary power failure exceeding 2 cycles of power frequency occur, the CPU detects the power failure and stops. The CPU restarts upon recovery from the power failure. The contents of the respective timers, auxiliary relays and output relays before the power failure are cleared.

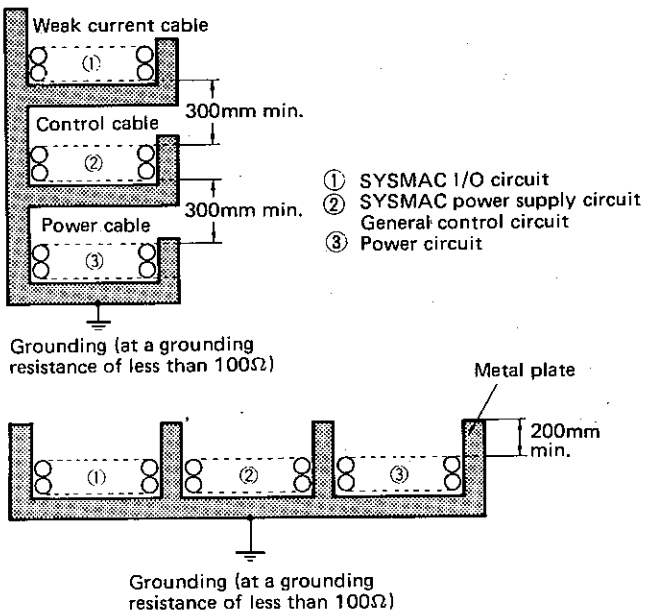
CPU RUN/STOP Timing Chart



   c. Automatic reset
      The SYSMAC-M1R will automatically resume its operation after the supply voltage (more than 85%) is restored.

8.6 External Wiring

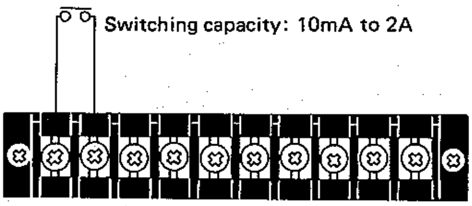
1. Be sure to process the input/output lines of the SYSMAC-M1R separately from other control lines. (Do not share the conductors of the I/O cable with others.)
2. To process the cables for the SYSMAC-M1R with power cables rated at 400V 10A max. or 220V 20A max.:
   a. Be sure to provide a minimum distance of 300mm between both cables when their racks are paralleled.
   b. Be sure to screen them with grounded metal plate when both cables are placed in the same duct at the termination process of the cable laying work.



8.7 Hints on Use of Externally Operated I/O Relay

- **CPU failure output**

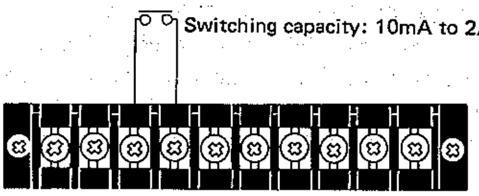
  This output is a no-voltage contact (SPST-NO) output which is activated (ON) when a CPU failure or I/O bus failure occurs while the CPU is in the RUN mode.



- **RUN output**

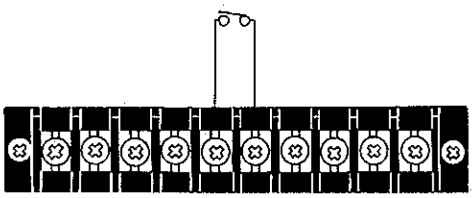
  This output is a non-voltage contact (DPST-NO) output which is activated (ON) while the CPU is in the RUN mode. The output, however, is inactivated (OFF) whenever one of the following conditions occur:

  (1) When a CPU or I/O bus failure occurs.
  (2) When mode other than RUN is set.
  (3) When a momentary power failure occurs.
  (4) When the supply voltage drops below 85% of the rated voltage.
  (5) When the fuse in the CPU has blown out.



- **OUTPUT INHIBIT input**

  When the OUT INHIBIT input terminals are short-circuited (i.e., closed), the output relays release and when the input terminals are disconnected (i.e., open), the output relays operate.



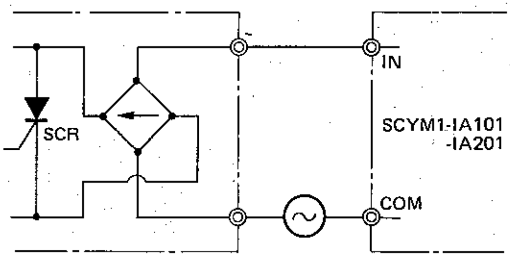
When contacts are open: All output relays are in the ON state.
When contacts are closed: All output relays are in the OFF state.

8.8 Interfacing Solid-state Input Devices

When using solid-state input devices, pay attention to the output forms of solid-state input sensors.
Examples of interfacing Control I/O (C I/O) units of SYSMAC-M1R with OMRON proximity or photoelectric switches are shown below.

8.8.1 Type SCYM1-IA101/-IA201

1. AC two-wire system type: This type can be used conditionally.

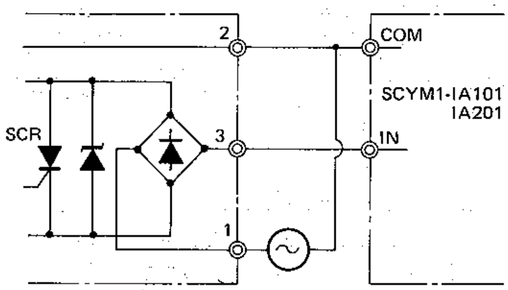


Applicable models
- OMRON proximity switches

Type	at AC110/120V	at AC220/240V
TL-X□Y□ series, TL-N(F)□MY□, TL-M□Y1, TL-LY50, E2K-C25MY series	O	O
TL-XY(B)□(M) series, TL-X□Y□-50, E2P-N15Y□	O	X
TL-YS(B)10(R) series, E2M-□Y□ series	X	X

O: Can be used. X: Cannot be used.

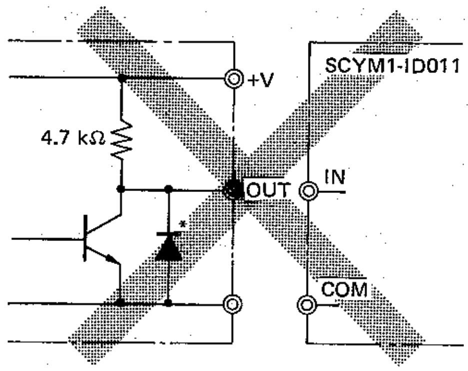
2. AC three-wire system type: This type can be used.



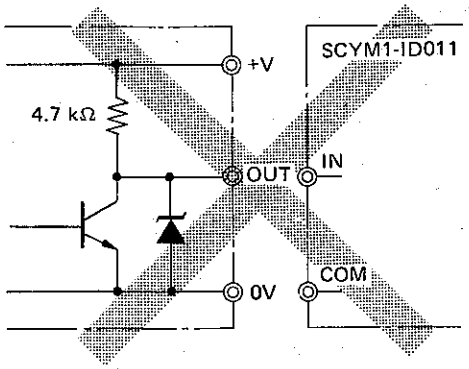
Applicable models
- OMRON photoelectric switches
  Type E3A-□Z□ series

8.8.2 Type SCYM1-ID011

1. NPN output type:
   This type cannot be used.

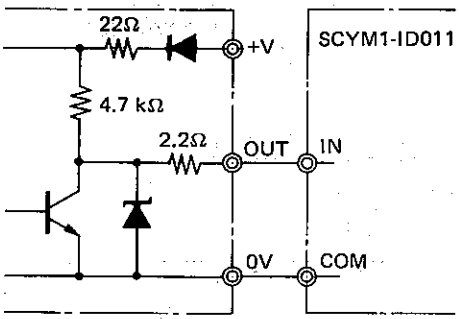


Models not applicable
- OMRON proximity switches
  Type TL-X□(M) series
  (+V: DC 10 to 14V)
  Type TL-G□/-Q□ series
  (+V: DC 12V)
  NOTE: * Type TL-G□ is not equipped with a diode.
  Type TL-Q□ incorporates a capacitor (0.01μF) instead of a diode.



Models not applicable
- OMRON proximity switches
  Type E2M-□□ series
  (+V: DC 12V)

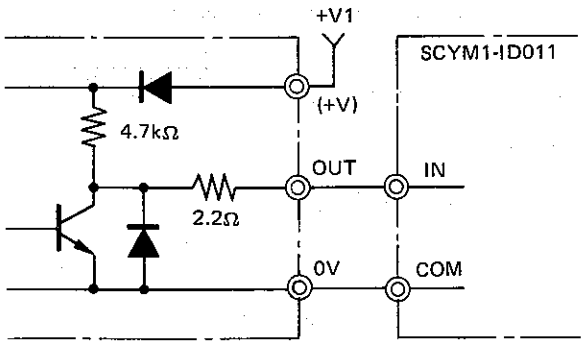
This type can be used conditionally.



Condition of use: +V at DC 15V min.

Application models
- OMRON proximity switches
  Type E2K-C25ME□ series
  (+V: DC 10 to 40V)

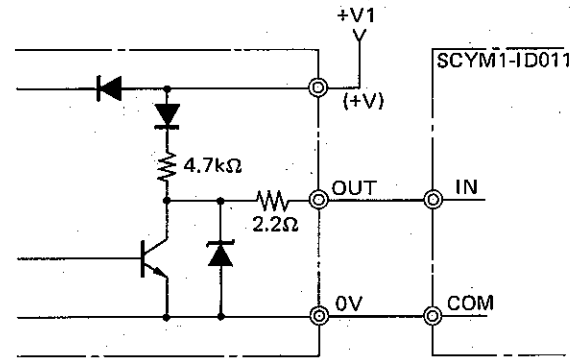
This type can be used conditionally.



Condition of use: +V1 at DC 15 to 30V
(+V at DC 10 to 30V)

Applicable models
- OMRON proximity switches
  Type TL-N(F/H)□ME□
  [+V1: DC 15 to 30V
  (+V: DC 10 to 30V)]

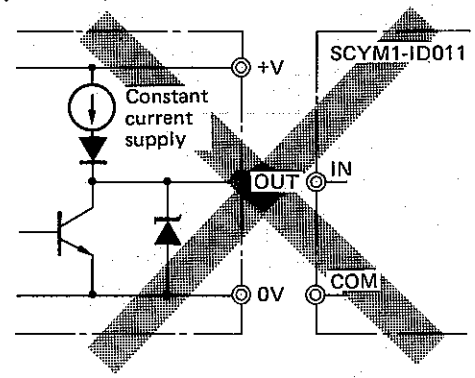
This type can be used conditionally.



Condition of use: +V1 at DC 15 to 30V
(+V at DC 10 to 30V)

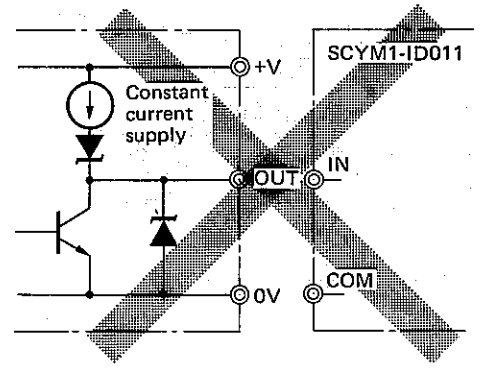
Applicable models
- OMRON proximity switches
  Type TL-M□E□
  [+V1: DC 15 to 30V
  (+V: DC 10 to 30V)]

This type cannot be used. (Use Type SCYM1-ID022 Input Unit.)



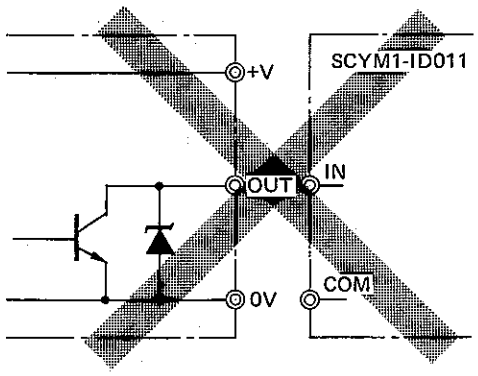
Models not applicable
- OMRON proximity switches
  Type TL-X□E□ series
  (+V: DC 10 to 40V)

This type cannot be used. (Use Type SCYM1-ID022 Input Unit.)

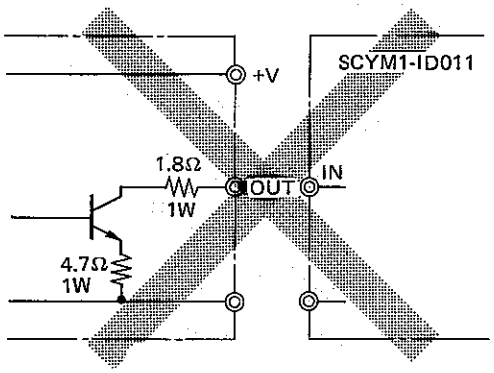


Models not applicable
- OMRON photoelectric switches
  Model E3S series
  Model E3S-L series
  Model E3S-G series
  Model E3S-X series
  Model E3N series
  (+V: DC 12 to 24V)

2. NPN open collector type:
This type cannot be used. (Use Type SCYM1-ID022 Input Unit.)

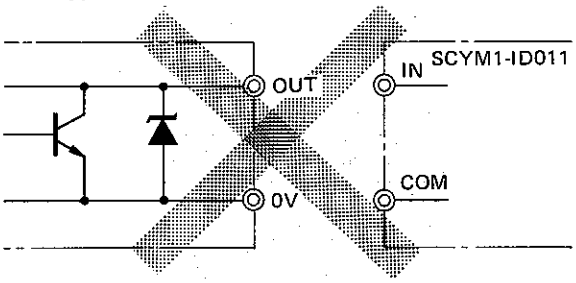


Models not applicable
- OMRON proximity switches
  Type TL-XP□(M) series
  (+V: DC 10 to 30V)
  Type E2M-□P□ series
  (+V: DC 24V)



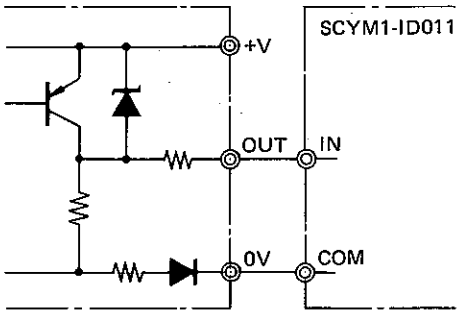
Models not applicable
- OMRON proximity switches
  Type TL-LP50
  (+V: DC 10 to 30V)

This type cannot be used.

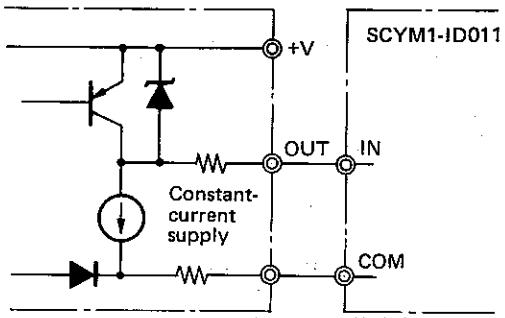


Models not applicable:
- OMRON proximity switches
  Type TL-XD

3. PNP output type:
This type can be used conditionally.



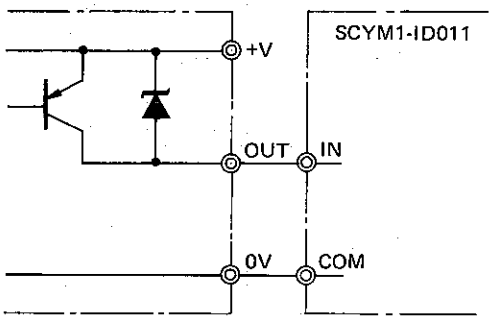
Applicable models
- OMRON proximity switches
  Type E2K-C25MF□ series
  (+V: DC 10 to 40V)



Condition of use: +V at DC 12V max.

Applicable models
- OMRON proximity switches
  Type TL-X□F□ series
  (+V: DC 10 to 40V)

4. PNP open collector type:
This type can be used conditionally.



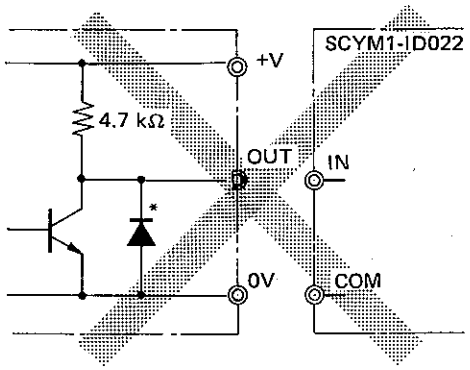
Condition of use: +V at DC 12V max.

Applicable models
- OMRON proximity switches
  Type TL-XP□(M)P
  (+V: DC 10 to 30V)

8.8.3 Type SCYM1-ID022

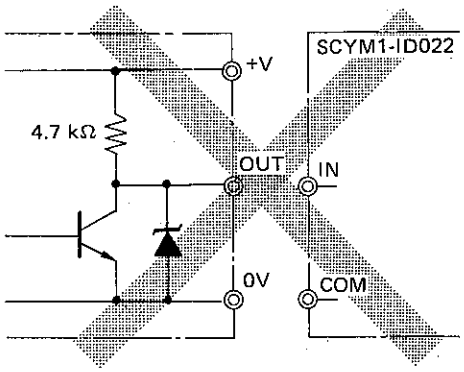
1. NPN output type:

This type cannot be used.



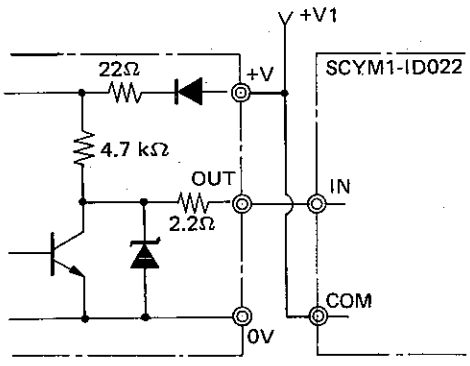
Models not applicable
- OMRON proximity switches
  - Type TL-X□(M) series (+V: DC 10 to 14V)
  - Type TL-N□/-H□/-F□ series (+V: DC 12V)
  - Type TL-G□/-Q□ series (+V: DC 12V)

NOTE: * Type TL-G□ is not equipped with a diode. Type TL-Q□ incorporates a capacitor (0.01μF) instead of a diode.



Models not applicable
- OMRON proximity switches
  - Type E2M-□□ series (+V: DC 12V)

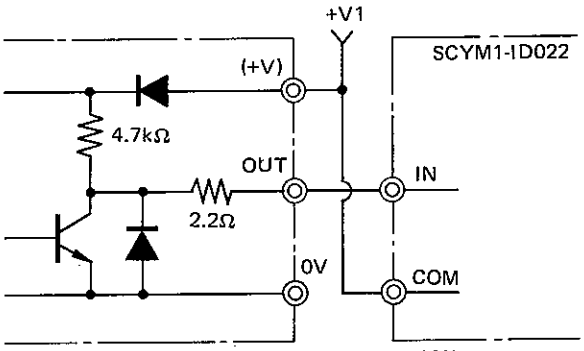
This type can be used conditionally.



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$

Applicable models
- OMRON proximity switches
  - Type E3K-C25ME□ series (+V: DC 10 to 40V)

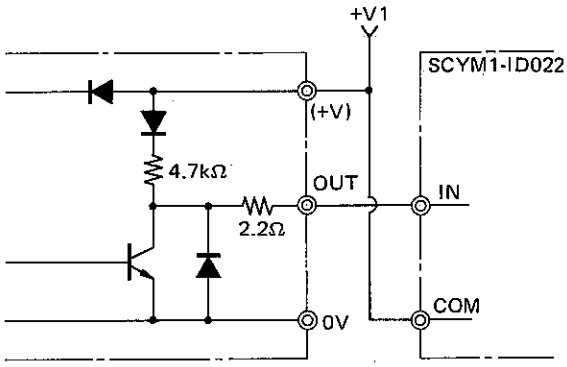
This type can be used conditionally.



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$ (+V at DC 10 to 30V)

Applicable models
- OMRON proximity switches
  - Type TL-N(F/H)□ME□ [+V1: DC 24V +10%, −15% (+V: DC 10 to 30V)]

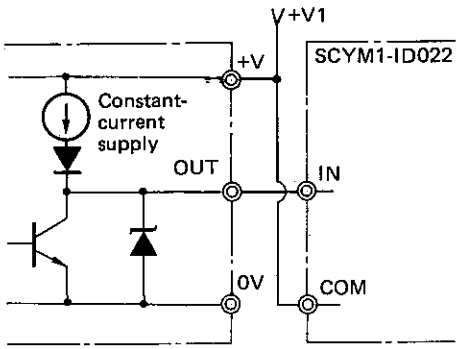
This type can be used conditionally.



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$ (+V at DC 10 to 30V)

Applicable models
- OMRON proximity switches
  - Type TL-M□E□ [+V1: DC 24V +10%, −15% (+V: DC 10 to 30V)]

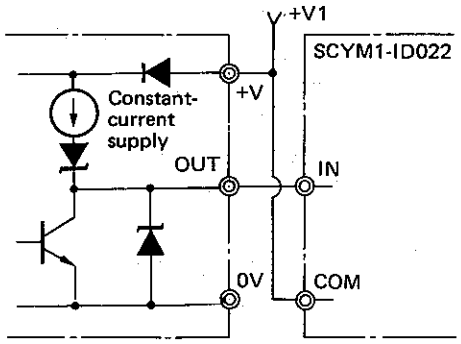
This type can be used conditionally.



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$

Applicable models
- OMRON proximity switches
  - Type TL-X□E□ series (+V: DC 10 to 40V)

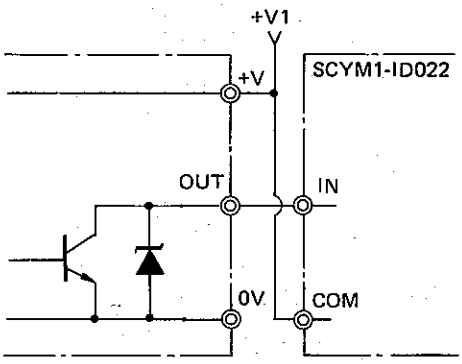
This type can be used conditionally.



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$

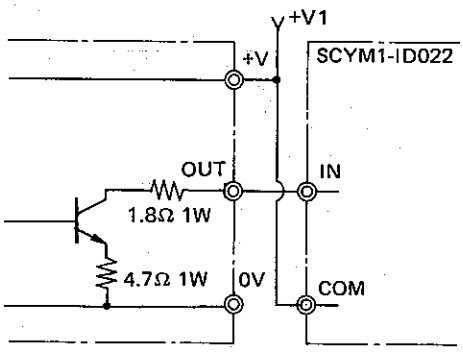
Applicable models
- OMRON photoelectric switches
  - Model E3S series
  - Model E3S-L series
  - Model E3S-G series
  - Model E3S-X series
  - Model E3N series
    (+V: DC 12 to 24V)

2. NPN open collector type:
This type can be used conditionally.



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$

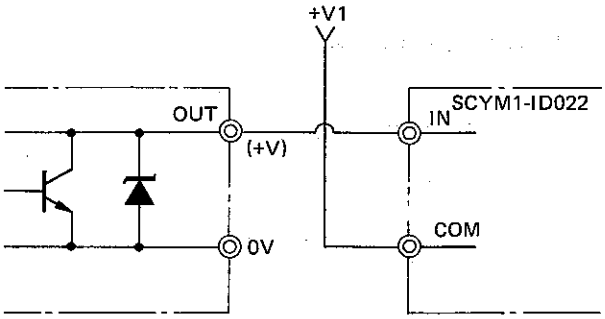
Applicable models
- OMRON proximity switches
  - Type TL-XP□(M) series
    (+V: DC 10 to 30V)
    Type E2M-□P□ series
    (+V: DC 24V)



Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$

Applicable models
- OMRON proximity switches
  - Type TL-LP50
    (+V: DC 10 to 30V)

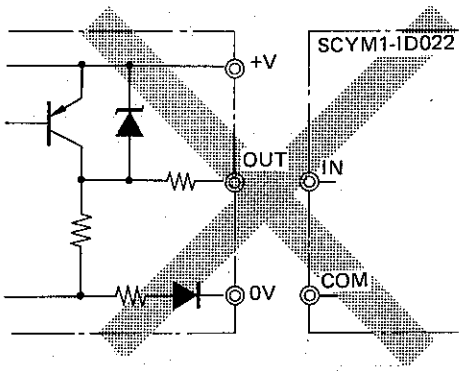
This type can be used conditionally.



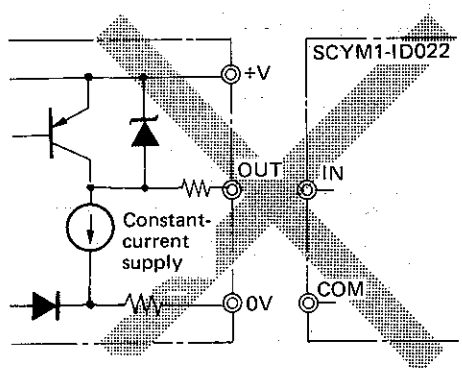
Condition of use: +V1 at DC 24V $^{+10\%}_{-15\%}$
(+V at DC 8 to 40V)

Applicable models
- OMRON proximity switches
  - Type TL-XD
    [+V1: DC 24V +10%, −15%
    (+V: DC 8 to 40V)]

3. PNP output type:
This type cannot be used. (Use Type SCYM1-ID011 Input Unit.)

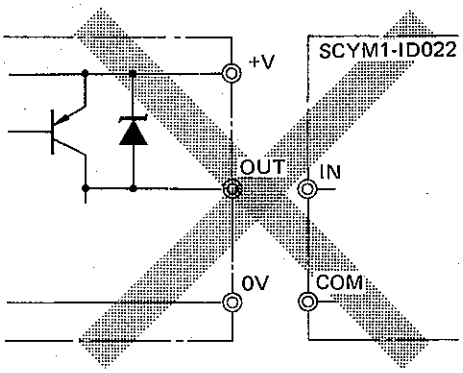


Models not applicable
- OMRON proximity switches
  - Type E2K-C25MF□ series
    (+V: DC 10 to 40V)



Models not applicable
- OMRON proximity switches
  - Type TL-X□F□ series
    (+V: DC 10 to 40V)

4. PNP open collector type:
This type cannot be used. (Use Type SCYM1-ID011 Input Unit.)

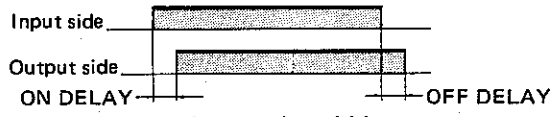


Models not applicable
- OMRON proximity switches
Type TL-XP□P(M) series
(+V: DC 10 to 30V)

8.9 Hints on Use of Control I/O [C I/O] Units

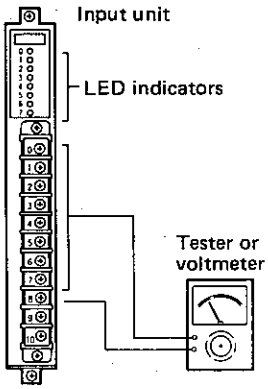
8.9.1 Input units

1. Input signal width
The width of a readable input pulse varies depending on the number of program steps.



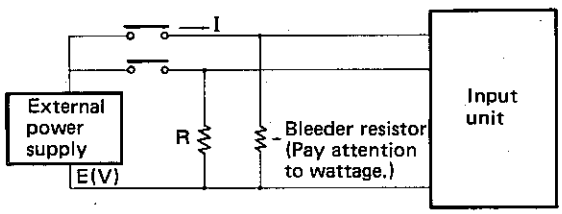
Max. input pulse width
= Number of steps x 0.1msec
+ 3msec + Input unit delay time

2. LED indicators
On the front panel of the input unit, an array of LEDs are provided to indicate the operating state of each external device connected. Since the LEDs illuminate at a voltage lower than the rated voltage, be sure to check the voltage when the LEDs operate unstably.



Refer to the specifications of each input unit for the voltages between respective terminals 0 through 7 and COM terminal 8.

3. Bleeder resistor
Only the input current specified for the input unit flows into the contacts connected to the input unit. When contact failure is likely to occur due to insufficient input current, or when there is a possibility of a large induced voltage from the external wiring, it is recommended to insert a bleeder resistor in the external circuit of the input unit.



- Resistance

$$R = \frac{E(V)}{\text{Contact current I (A)} - \text{Input current (A)}} \ (\Omega)$$

- Wattage

$$W1 = \left(\frac{E^2}{R}\right) \times 2 \ (W)$$

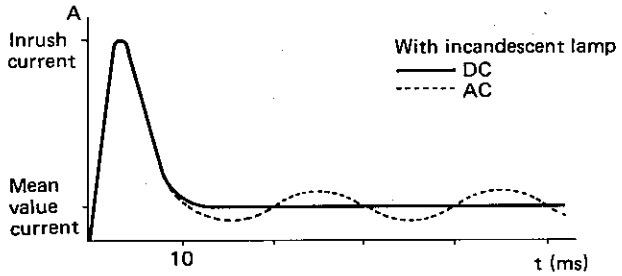
8.9.2 Output units

1. Maximum switching capacity
The following ratings are guaranteed within the specified temperature range. Note that use of any output unit beyond the specified temperature range may result in damage to its internal elements or shortening of its service life.

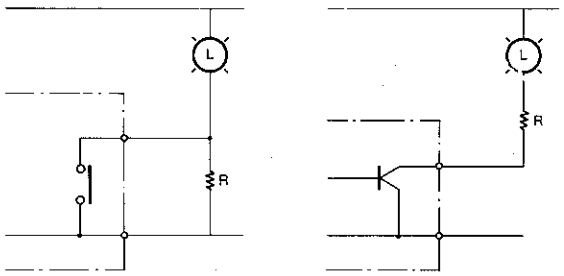
Type	Maximum voltage	Maximum carry current	Maximum inrush current *2
OC203	AC 250V	2A	6A
	DC 26.4V	2A	3A
OA201	AC 242V	1A	8A *1
OD041	DC 52.8V	0.5A	4A

NOTES: *1. A maximum 4 outputs may be turned on simultaneously.
*2. 10msec max. Repeated for more than 1sec.

2. Lamp load and inrush current
When a lamp is illuminated, a current 15 to 20 times the steady-state current flows into the lamp. In AC ratings, the steady-state current is indicated by a root mean square (rms) value. To figure out its peak value, I peak = $\sqrt{2}$ Irms should be taken into account.
With an AC lamp load, when an output unit with zero cross function is employed for switching the lamp load, the inrush current of the lamp load reduces to 1/2 to 1/3 of that when AC peak current is applied.



3. How to reduce inrush current (with SYSMAC M1-OC203 output units)
When switching a lamp load greater than the specified ratings, the inrush current of the lamp load must be reduced by either of the following two methods.



Bleeder method　　Limited resistance method

a. Bleeder method (i.e., to flow bleeder current by inserting a bleeder resistor)
This method is not so effective for the Type OA201 output unit in which some leakage current is inevitable. For Type OC203 output units, a bleeder resistor is inserted to cause a leakage current corresponding to 1/10 to 1/20 of the steady-state current to flow into the lamp load. As the result, these output units can be applied to the loads 50% larger than the maximum permissible lamp loads described above.

b. Limited resistance method (i.e., to insert a current-limiting resistor in series with lamp)
In this method, the inrush current is limited by the current governed by resistor R. However, note that the greater the resistance value, the greater the current consumption by the resistor, which in turn reduces the voltage to be applied to the lamp.

4. AC solenoid load and starting current
The starting current that flows through the AC solenoid is severalfold to several ten-fold larger than the holding current.
It may also continue for several 10msec to several 100msec. Therefore, use the solenoid whose 1/2 of the starting current is less than the maximum inrush current shown in the maximum switching capacity of each output unit.

Type	Max. inrush current
OC203	3A max.
OA201	4A max.

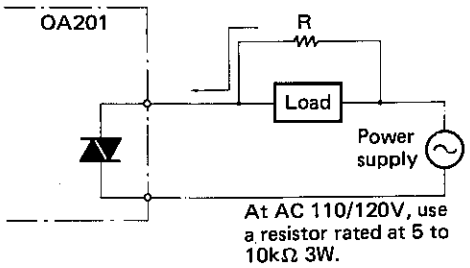
5. Electromagnetic switch load and capacity
There exists no problem when the output unit is used to switch an electromagnetic switch directly if the switch is of miniature type. As a guide to determine whether or not the output unit can switch the load, divide the current value obtained from the capacity of the electromagnet before energization by $\sqrt{2}$. If the result is less than the maximum inrush current described before in maximum switching capacity, it is possible to switch the load with the output unit.

Operating coil / Type	Capacity of electromagnet before energization (at start)	
	AC 110/120V	AC 220/240V
OC203	420VA max.	840VA max.
OA201	560VA max.	1120VA max.

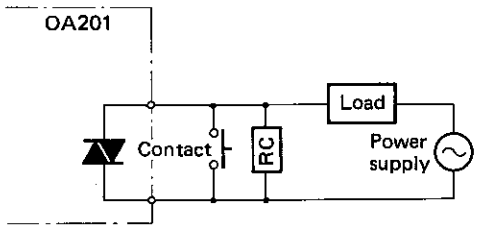
6. Effects of leakage current on loads
The leakage current of each output unit is as shown in the following table. With the Type OD041, no specific problem exists. With the Type OA201, however, the output relays may not release properly depending on the size of the load to be switched. Therefore, when using the output unit, pay attention to this point.

OA201	OD041
3.3mA at 110V, 3.6mA at 120V	100μA max.

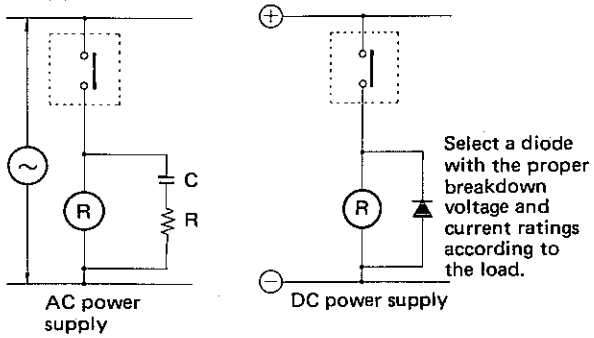
7. Method to alleviate effects of leakage current
When a low-capacity load is to be connected to the Type OA201 output unit, insertion of a bleeder resistor in parallel with the load help minimize the effects of leakage current on the load.



8. Switching of load with OA201 and contact
Avoid arrangement of a contact circuit in parallel with the Type OA201 output unit as shown below, or the internal elements of the output unit may be damaged. If such circuit arrangement is unavoidable, be sure to insert an RC network in parallel with the contact.

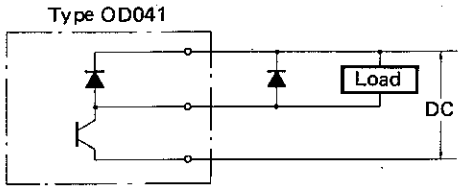


9. Countermeasures against surges
The SYSMAC-M1R is provided with adequate measures to prevent the output unit from malfunctioning due to surging, for example, when switching a lamp load. However, take note that a surge voltage of several 1,000 volts may occur in electromagnetic switches, AC solenoids, etc.
For general-purpose relay such as OMRON Models MY and LY, no countermeasure against surges is required. For larger loads than these relays, the following countermeasures are recommended. It should be noted that when either of the countermeasures is provided, the release time of the relay will be delayed slightly.



C: 0.5μF ±20% max. Non-polarity
Breakdown voltage 1500V min.
R: 50Ω ±30% max. 0.5W

In relay output type units such as Type OC203, the installation of a surge suppressor is recommended in view of output contact protection.
Transistor output type unit Type OD041 has a built-in diode for its protection against surges. However, if the external wiring of the output unit is extended (to more than 3m), the built-in diode may not be able to function effectively. Therefore, insertion of another diode is recommended on the load side.



Since triac output type unit Type OA201 turns on in the vicinity of zero volt and turns off in the vicinity of zero current, the generation of surges can be reduced to a great extent. Because of this feature, the output unit requires no surge suppressor.

10. Minute load switching
Since the output relays incorporated in relay output type units such as OC203 are for power switching, their contact construction is not suitable for switching very small loads. Therefore, these output units are not strongly recommended for minute load switching.

- Minimum permissible load

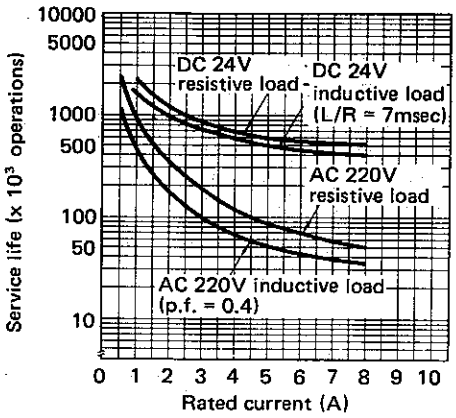
OC203	DC 5V 10mA

11. Service life of relay output type unit
The service life of each output unit is as shown in the following table.

Type	AC load	DC load	Mechanical life
OC203	200,000 operations	900,000 operations	2,000,000 operations

Note: Both AC and DC are rated loads.

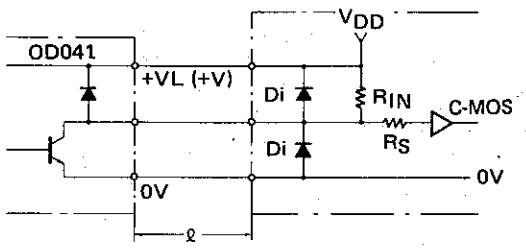
If a surge suppressor is mounted to the load to be switched, or if the load is smaller than the rated load, the service life may be extended severalfold to several ten-fold longer than the rated service life.
In addition to the service life of the contacts, the relay coil characteristics will also deteriorate. Therefore, it is recommended to replace each output relay every 3 to 5 years even if the number of switching operations of the relay has not reached the rated life. (Refer to the following service life curve.)



12. Maximum switching frequency
With the relay output type units, the built-in output relays are limited for use according to their maximum switching frequency. Type OC203 has a switching frequency of 30 operations max. per minute (with a minimum time interval of 2sec for switching).

13. Connection with ICs such as TTL, C-MOS, etc.
Since the relay output type units are intended for switching small loads, they are not suitable for connection with ICs. Some transistor output type units, however, can be connected to ICs.
The saturation voltage of the output transistor is as high as 1.2 to 1.5V, so the output unit cannot be connected to a TTL whose V_{IL} ("0" input voltage) is 0.8V.
B series C-MOS's (Motorola MC14XXXB, etc.) has a V_{IL} of 1.5V max. (at V_{DD} = 5V). Therefore, the output transistor can be connected with any of B series C-MOS's.
The UB series C-MOS's (Motorola MC14XXXUB, Toshiba TCXXXUBP, etc.) has a V_{IL} of 2V max. (at V_{DD} = 10V), the output transistor can also be connected with any of the UB series.

	TTL	C-MOS B series	C-MOS UB series	Applicable Unit
V_{DD} = 10 ~ 15V	X	○	○	OD041 OD042



- Di is a diode (Reverse-breakdown voltage: 30V min. / Capacity: 120mA min.)
- R_S are:

V_{DD}	10V	15V
R_S	10kΩ	15kΩ

- ℓ is 3m max.
- R_{IN} is determined as follows. $\frac{V_{DD}}{5 \text{ to } 10}$ (kΩ)

9. Maintenance and Inspection

To sustain the proper system operation at all times, it is necessary to inspect the SYSMAC-M1R daily. If any trouble occurs in the SYSMAC-M1R, how the system should be protected and how soon it can be recovered from the failure become important. In this chapter, the items to be inspected on the SYSMAC-M1R and the actions to be taken if the SYSMAC-M1R fails are described.

9.1 Inspection

To make the most of the functions of the SYSMAC-M1R under the best condition, it is necessary to inspect the SYSMAC-M1R daily or periodically.

■ INSPECTION ITEMS

The SYSMAC-M1R employs semi-conductors as its main component elements and has few or no supplies with a limited service life. However, the semi-conductors may deteriorate depending on the environmental conditions and must therefore be inspected periodically. The standard inspection cycle is 6 months to 1 year. According to the environmental conditions, it is recommended to advance the date of inspection. As a result of the daily or periodical inspection, if the SYSMAC-M1R is found to be outside the criteria in the following table, be sure to correct the SYSMAC-M1R so that it falls within the prescribed criteria.

No.	Inspection item	Particulars of inspection	Criteria
1	AC power supply (a) Voltage (b) Fluctuation	(1) Is the rated voltage available when measured at the AC input terminal block?	AC 110, 120, 220, or 240V +10%, −15%
		(2) Does a momentary power failure occur frequently or is there any sharp rise or drop in the supply voltage?	The supply voltage must be within the permissible fluctuation range described above.
2	Environmental conditions (a) Ambient temperature (b) Humidity (c) Vibration (d) Dust, etc.	Are the temperature and humidity within the respective range? (When the SYSMAC-M1R is installed in a control panel, the temperature within the panel may be regarded as the ambient temperature of the programmable controller.)	(a) 0 to +50°C (b) 30 to 90% RH (c) Must be free from vibration. (d) Must be free from dust.
3	Power supply of expansion I/O rack (a) Voltage (b) Ripple	Are the voltage and ripple within the operating range when measured at the terminal board of each I/O rack?	Must conform with the specifications of each I/O unit.
4	Mounting conditions	(1) Are the CPU rack and expansion I/O racks secured firmly?	The mounting screws must not be loose.
		(2) Are each I/O units and interface unit fixed firmly?	Each I/O base unit and its interface unit must not be loose.
		(3) Is the I/O connecting cable inserted completely?	The connecting cables must not be loose.
		(4) Is there any loose screw in the external wiring?	The screw terminals must not be loose.
		(5) Is there any broken cable in the external wiring?	The external wiring must be free from any abnormalities in appearance.
5	Service life	(1) Output relays in the I/O units	Replace with new ones if defective.
		(2) Battery	1 year

CAUTION:
Be sure to turn off the power before replacing any unit of the SYSMAC-M1R.

■ NOTES ON INSPECTION

1. If a defective unit is discovered and replaced, confirm whether or not the replaced unit is abnormal.
2. In the event of a faulty contact of the cable, wipe the connector pins with a clean all-cotton cloth moistened with industrial alcohol. Be sure to plug in the flat cable after removing the cloth waste.

■ TOOLS AND TESTING EQUIPMENT REQUIRED FOR MAINTENANCE

In the maintenance of the SYSMAC-M1R, the following tools and testing equipment will facilitate the daily or periodic inspection of the programmable controller.

1. Tools and testing equipment recommended as mandatory equipment
   - Screwdrivers (Phillips and round-blade)
   - Tester or digital voltmeter
   - Industrial alcohol and all-cotton cloth
2. Measuring instruments recommended only if required.
   - Synchroscope
   - Pen-recording oscilloscope

■ MAINTENANCE PARTS

1. I/O unit
   If the SYSMAC-M1R fails, its repair is impossible without any spare parts no matter how early the trouble is discovered. So, it is recommended to have at least one I/O unit as a spare part.
2. Battery (Type SCYM1R-BAT80)
   In general, the service life of a battery is regarded as the time when the terminal voltage of the battery is reduced to 2.5V. When the battery has been discharged, "BATTERY FAILURE" indicator illuminates. Be sure to replace the battery with a new one within a week after the "BATTERY FAILURE" indication. The life of the built-in battery is considered to be 2 years.
3. Fuses
   AC power fuse: Rated at 3A
   DC 5V power fuse: Rated at 10A

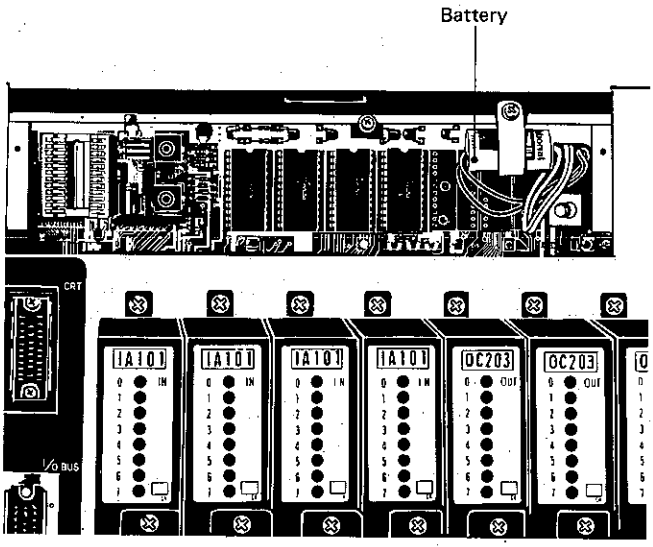
9.2 Replacement of Battery

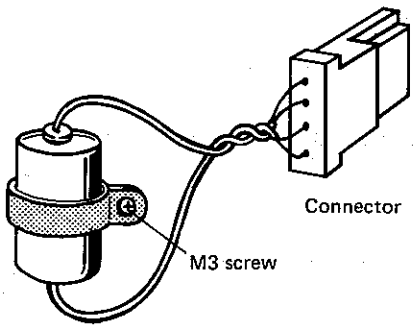
Be sure to replace the battery within 5 minutes.

- **Procedure:**

1. Prepare the replacement battery.
2. Turn off the AC power.
3. Open the door located at the upper part of the I/O section in the CPU rack.

   NOTE: When the AC power is not ON at the time of the battery replacement, first apply the AC power for more than 10sec and then turn it off.



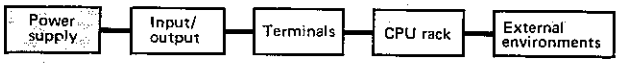


4. Remove the M3 screw securing the battery and unplug the battery connector.
5. Plug in the connector of the new battery, and then secure the new battery with the M3 screw.
6. Close the door and secure it with the screws.
7. When the AC power is applied, the battery starts operating.

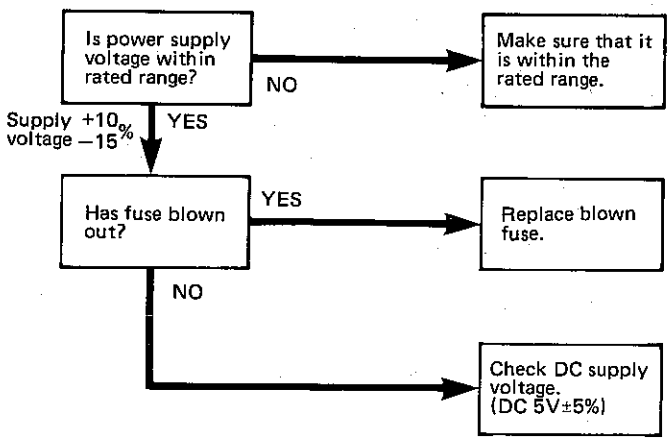
9.3 Troubleshooting

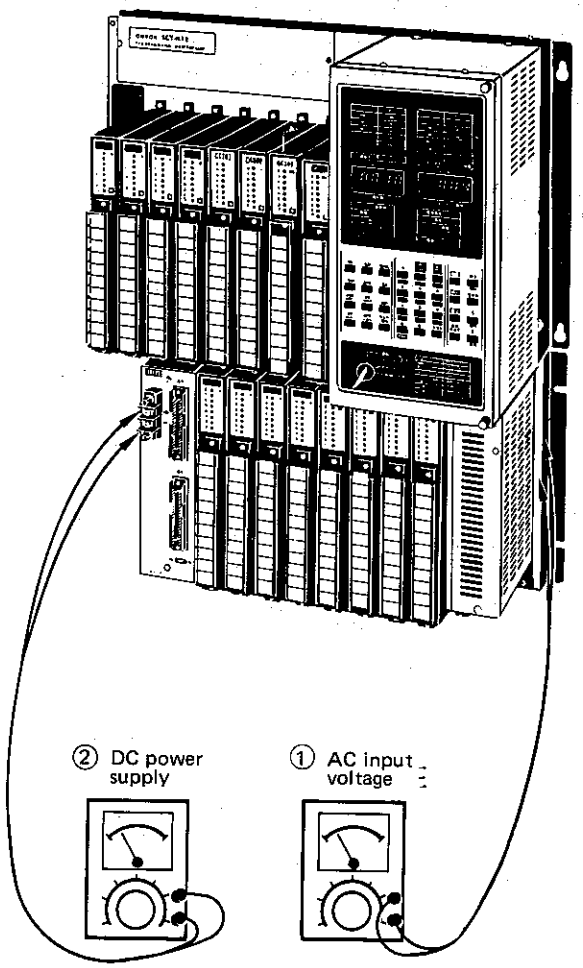
If any abnormality occurs in the SYSMAC-M1R, thoroughly grasp the condition of trouble, check whether the symptom is reproducible or is caused through relationship with other equipment, and then follow the troubleshooting flowcharts shown below.

■ POWER SUPPLY

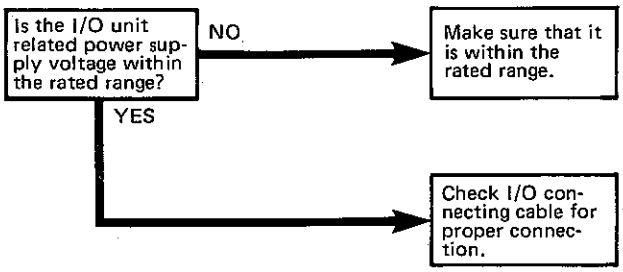


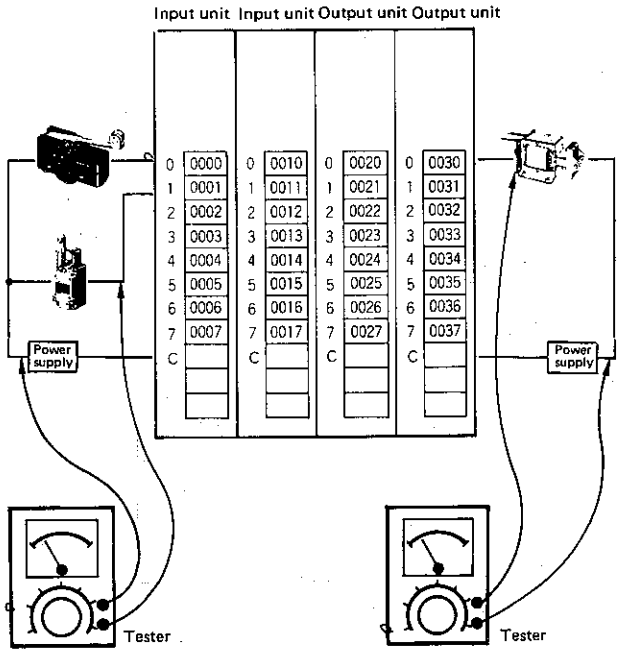
1. Main power supply check
   In this check, the AC power being supplied to the SYSMAC-M1R is confirmed if it is within the rated range (+10%, −15 of rated voltage).



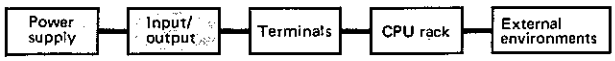


2. I/O unit related power supply check
The power supply for loads is connected to the terminals of each I/O unit. Should any abnormality occur in this power supply, the I/O device connected to the I/O unit will not operate.



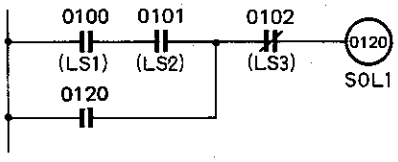


■ INPUT/OUTPUT UNIT

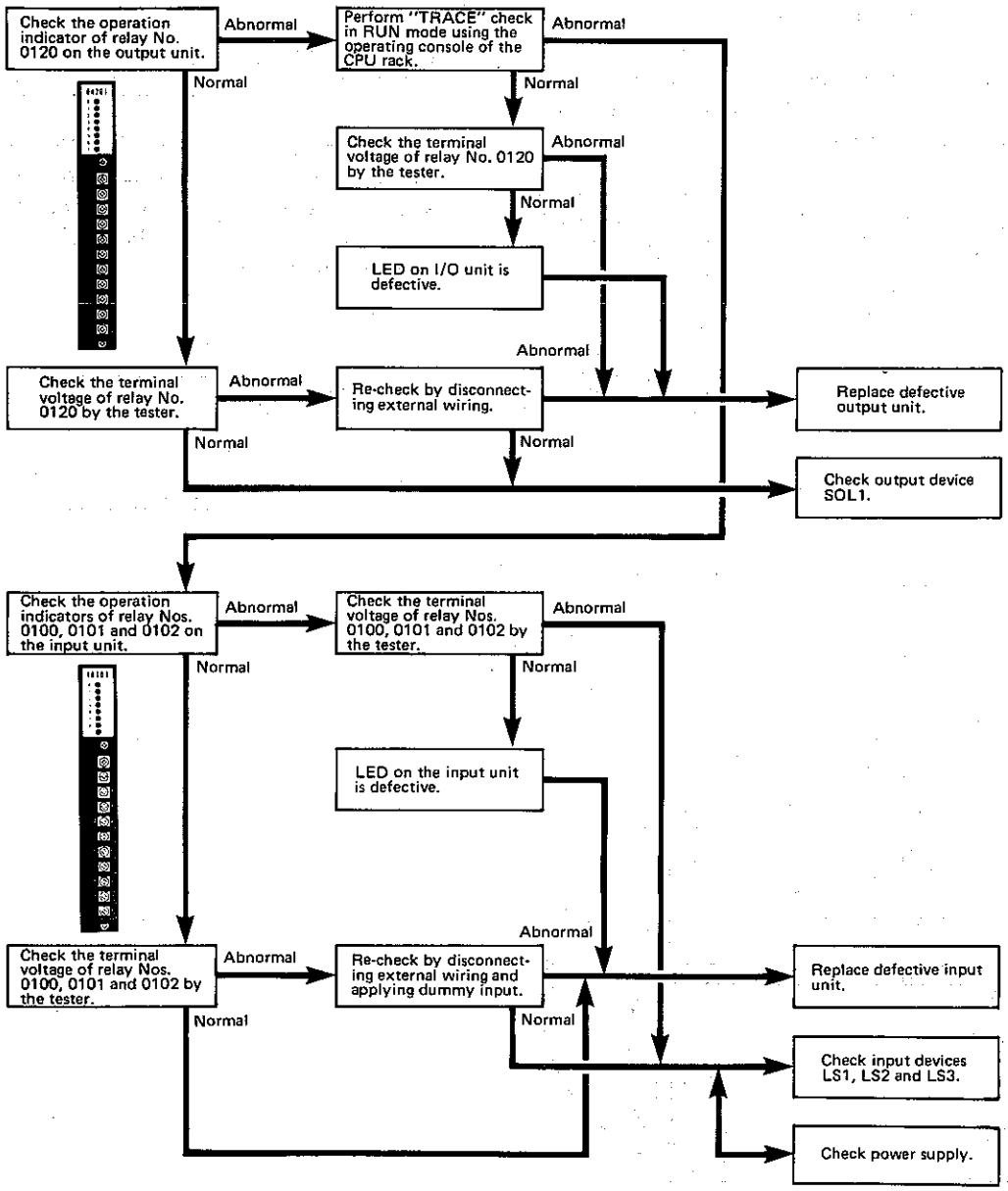


The following flowchart is indicated on the assumption that the maintenance spare parts are provided. If no spare part is provided, first check I/O devices thoroughly. The flowchart is illustrated based upon the circuit example shown below.

Circuit example



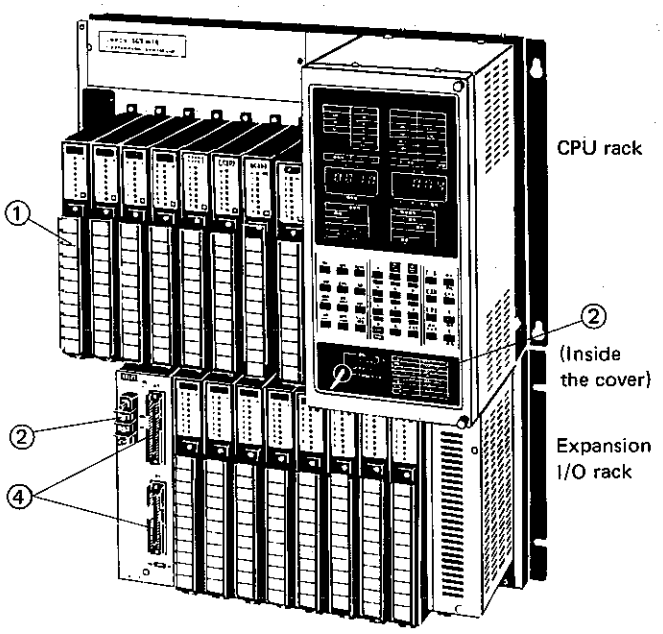
SOL1 malfunctions!!



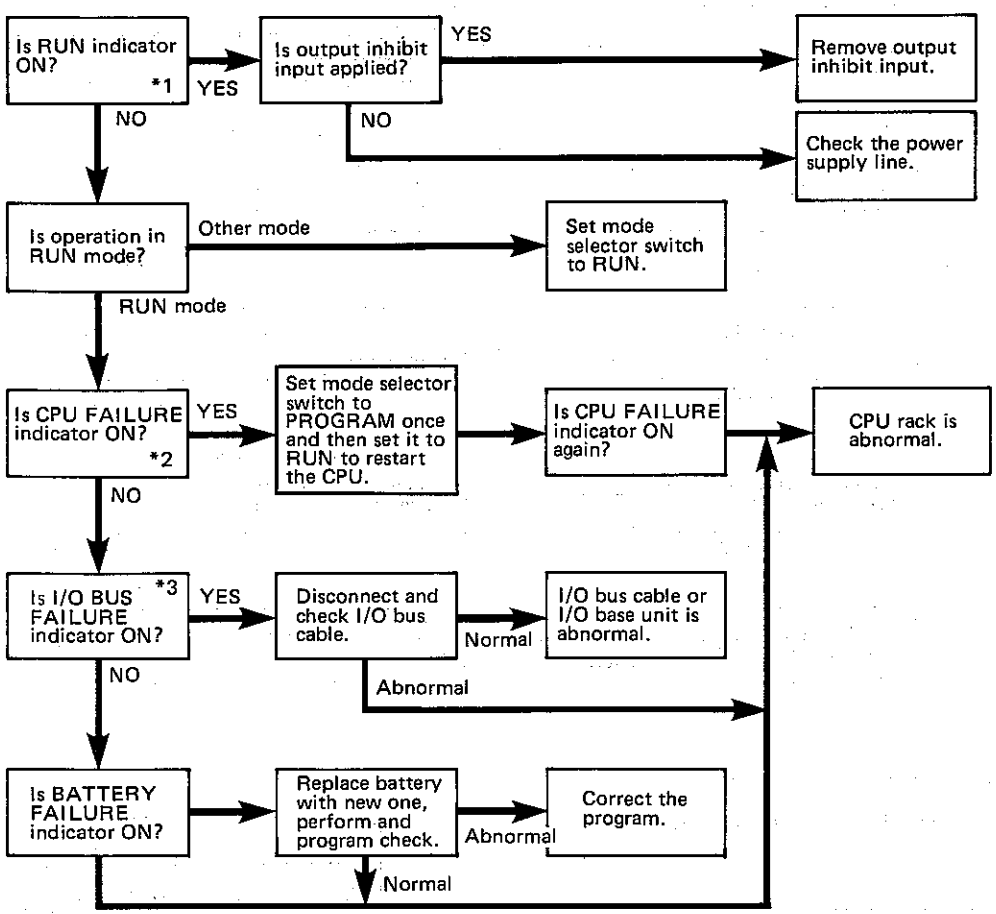
■ TERMINALS

Power supply — Input/output — Terminals — CPU rack — External environments

① Check each I/O unit for loose terminals.
② Check the power supply terminals for loose connection.
③ Check each unit for loose mounting screws.
④ Check the I/O connecting cable for proper mounting.



■ CPU RACK

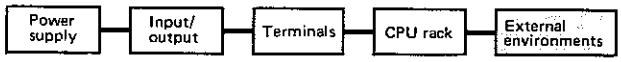


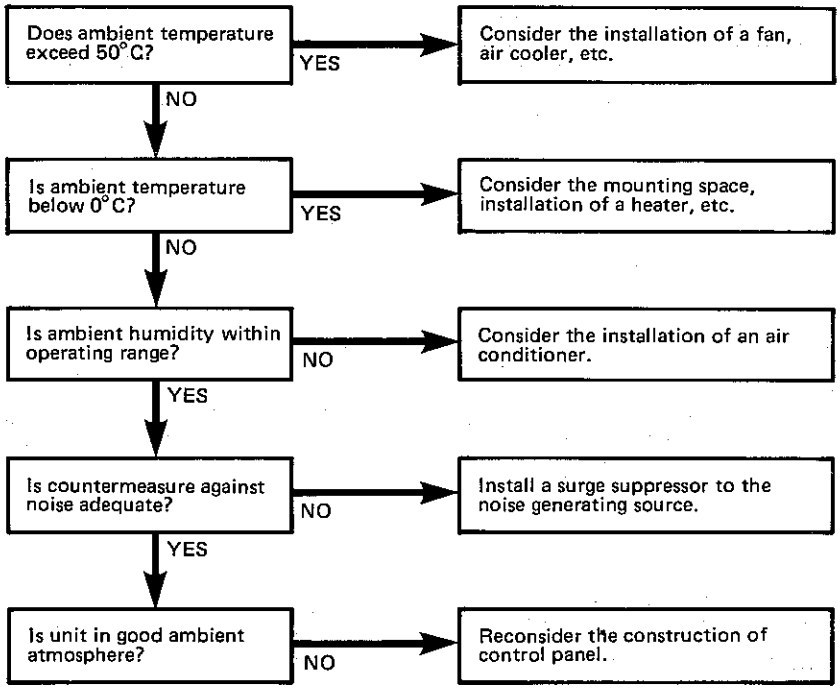
NOTES: *1. When the AC input supply voltage drops below 85% of the rated voltage, the SYSMAC-M1R detects the condition as a power failure. Even if a momentary power failure occurs, but it is restored within 1 cycle, the SYSMAC-M1R ignores the power failure and continues operating.
If a momentary power failure continues for more than 2 cycles, SYSMAC-M1R detects the condition as a power failure and resets its operation.
If a momentary power failure of 1 to 2 cycles occurs, which is in an unstable area, the SYSMAC-M1R may continue or reset its operation.
Once the power failure is detected, even if the power supply is returned to normal, it takes about 1sec for the SYSMAC-M1R to reset. During this time, the RUN output of externally operated relay is in the OFF state. Therefore, all outputs from the output units also turn OFF. The RUN output turns OFF when a CPU failure (watchdog timer) or I/O bus failure occurs. Should the RUN output be used in an emergency stop circuit, note the entire system operation may stop. So pay attention to the service life and contact ratings of this output relay.

*2. How to recover from CPU FAILURE (watchdog timer)
Restart the SYSMAC-M1R by changing the mode selector switch position from "RUN" to "PROGRAM" and then to "RUN" again.
NOTES:
1. If any abnormality still exists in the CPU rack, the CPU FAILURE indicator illuminates again.
2. The CPU FAILURE relay operates by depressing the CLEAR key or CLEAR DISPLAY key.

*3. How to recover from INPUT/OUTPUT FAILURE (I/O bus diagnostic error)
Restart the SYSMAC-M1R by changing the mode selector switch position "RUN" to "PROGRAM" and then to "RUN" again.
If the I/O FAILURE indicator illuminates again, check the SYSMAC-M1R as follows.
1. Disconnect the connecting cable between the CPU rack and the expansion I/O rack.
2. Connect other expansion I/O racks one by one successively (up to 3 racks).
3. Change the I/O connecting cable with that between other expansion I/O racks.
4. Change the I/O interface unit with that on other expansion I/O racks.

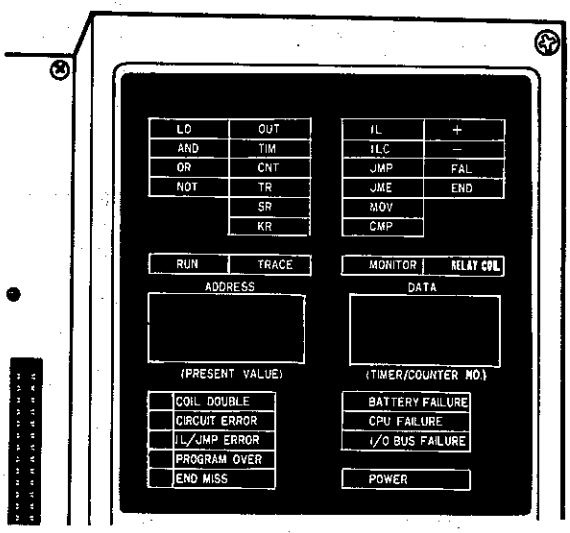
■ EXTERNAL ENVIRONMENT





9.4 List of Error Messages

An error message appears in the DATA display as shown on the right.



■ LIST OF ERROR MESSAGES

- The following error messages indicate the failure conditions occurred in the RUN mode.

NOTES:

1. The BATTERY FAILURE indicator will illuminate to alert the operator one week before the battery will be exhausted.
2. The buzzer will sound for about 1sec.
3. If the buzzer still sounds even after completion of the "Remedy" described in the above table, consult OMRON.

Item / Symptom	CPU rack								Output unit	Remedy
	RUN indicator	I/O BUS FAILURE indicator	CPU FAILURE indicator	BATTERY FAILURE indicator	Control I/O relay: RUN output	Control I/O relay: CPU FAILURE output	Special auxiliary relay No. 1374	Buzzer	Output indicator	
Momentary power failure	OFF	–	–	–	OFF	–	–	–	OFF	–
Voltage drop	OFF	–	–	–	OFF	–	–	–	OFF	–
Power supply: CPU rack fuse has blown	OFF	–	–	–	OFF	–	–	–	OFF	Three fuses are provided. Pay attention to the following: 1. 3A fuse (for AC input) on external terminal board Line filter, transfer or switching regulator element of power supply unit (PCB) is considered to be defective. • Check the supply voltage to see if the voltage indication by the voltage selector socket coincide with the actual input voltage? • Remove the power supply unit (PC board) for expansion I/O rack and I/O unit(s) in the CPU rack. • Check the wiring from the terminal board to the power supply unit. 2. 10A fuse (for +5V) on power supply unit (PC board) Check the wiring extending to the expansion I/O base unit since this fuse is for DC 5V. 3. 0.1A fuse (for L. OFF) on printed circuit board of power supply unit ... 0.1A (for L. OFF) Since this fuse is for load interrupt input, it cannot be repaired by the user. • Check if any voltage is not being applied to the load interruption input.
RUN mode → Other mode (Mode select switch)	OFF	–	–	–	OFF	–	–	–	–	–
CPU FAILURE (Watchdog timer)	OFF	–	ON	–	OFF	ON	–	ON (Note 2)	–	Check if the connector is not loose or is inserted incorrectly and check the 5V power supply. Then apply the power again.
BATTERY FAILURE (Note 1)	–	–	–	ON*	–	–	ON	–	–	Replace the battery within a week.
I/O BUS FAILURE	OFF	ON	–	–	OFF	ON	–	ON (Note 2)	–	Check the following points: • Is the connector of the I/O connecting cable inserted correctly? • Is the I/O connecting cable normal? Replace it with the cable between other expansion I/O racks. • Replace the interface unit with that on other expansion I/O rack.

NOTES: 1. The BATTERY FAILURE indicator will illuminate to alert the operator one week before the battery will be exhausted.
2. The buzzer will sound for about 1 sec.

9.5 Abnormal Symptom, Possible Cause and Corrective Action

- **CPU rack**

No.	Abnormal symptom	Possible cause	Corrective action	Remarks
1	Fuse blows repeatedly.	Pattern is short-circuited or damaged by burning.	Replace CPU rack.	Check the DC 5V wiring for I/O unit.
2	DC voltage output failure	Constant voltage circuit is defective.	Replace CPU rack.	—
3	"RUN output" contact of externally operated I/O relay does not release. (RUN indicator ON)	(1) Control I/O relay or power circuit is defective.	Replace CPU rack.	—
4	RUN indicator does not illuminate.	(1) DC voltage is not supplied. (2) Programming error (END instruction is missing.)	Replace CPU rack. Correct program.	—

- **Expansion I/O Racks**

No.	Abnormal symptom	Possible cause	Corrective action
1	Operation is not executed after specific relay No.	(1) Pattern is broken.	Check each bus line by buzzer.
		(2) Improper soldering	Resolder.
2	Abnormal relay Nos. of expansion I/O rack are in units of 8.	(1) Cable wiring is broken.	Check each bus line by buzzer.
		(2) Improper soldering	Resolder.
3	Output of a specific relay No. turns on.	(1) Improper soldering of connector	Check each bus line by buzzer.
4	All the relays of a specific I/O unit do not operate.	(1) Same as above	Check each bus line by buzzer.

- **Input units**

No.	Abnormal symptom	Possible cause	Corrective action
1	All input units do not turn on.	• Operation indicators (LEDs) are not illuminating. (1) External input voltage is not supplied or is low.	Supply the power. Raise the supply voltage.
		• Operation indicators (LEDs) are illuminating. (1) Signal level within unit is faulty.	Remove all the I/O units being used and insert them one by one to find a out defective unit.
2	All of specific input units do not turn on. (Example) 0010 ~ 0017	(1) Same as above	Same as above Replace defective input unit.
		(2) Screws of terminal board are loose.	Retighten terminal screws.
3	All of specific input units do not turn off.	(1) Gate circuit is defective.	Replace defective input unit.
		(2) External voltage is not supplied.	Apply the external power supply.
4	Input of a specific relay No. does not turn on. (Example) 0010	(1) Gate circuit is defective.	Replace defective input unit.
		(2) Screws of terminal board are loose.	Retighten screw terminals.
		(3) ON time duration of external input is short.	Adjust external device.
		(4) Input circuit (photocoupler, etc.) is defective.	Replace defective input unit.
		(5) Input relay No. is incorrectly assigned to the OUT instruction of the program.	Correct the program.
5	Input of a specific relay No. does not turn off.	(1) Contact of jack is defective.	Clean the contact part with alcohol-moistened cloth.
		(2) Input circuit is defective.	Replace defective unit.
		(3) Input relay No. is incorrectly assigned to the OUT instruction of the program.	Correct the program.
6	Relay No. of abnormal operation is in units of 8. (Example) 0000, 0010, 0020	(1) Data bus signal is faulty.	Remove all I/O units being used and insert them one by one to find the defective unit.
		(2) IC-RAM of CPU is defective.	Replace CPU rack.
7	Inputs turn ON and OFF irregularly.	(1) External input voltage is low.	Raise the external voltage.
		(2) Malfunction due to noise	Countermeasures against noise. • Install a surge suppressor. • Install a insulating transformer. • Wiring with a shielded cable
8	Input operation indicator does not illuminate. (Operation is normal.)	(1) LED indicator is defective.	Since this type of defect does not impede normal operation, repair it in spare time or at the next periodic inspection.

- **Output units**

No.	Abnormal symptom	Possible cause	Corrective action
1	All output units do not turn on.	(1) Load power supply is not applied.	Apply the load power supply. (Raise the voltage.)
		(2) Signal level within unit is defective.	Remove all the I/O units being used and insert them one by one to find the defect unit.
2	All of specific output units do not turn on. (Example) 0020 ~ 0027	(1) Same as 1 (1).	Same as above.
		(2) Screws of terminal board are loose.	Retighten screw terminals.
		(3) Contact of jack is defective.	Clean the contact with alcohol-moistened cloth.
		(4) Fuse is blown.	Replace defective fuse.
		(5) Internal circuit is defective.	Replace defective unit.
3	All of specific output units do not turn off.	(1) Contact of jack and connector is defective.	Clean with alcohol-moistened cloth.
		(2) Gate circuit is defective.	Replace defective unit.
4	Output of a specific relay No. does not turn on.	• Operation indicator (LED) is not illuminating. (1) ON time duration of output is short. (2) Relay Nos. of the OUT instruction in the program are in duplication. (3) Power circuit is defective.	Correct the program. Correct the program. Replace defective unit.
		• Operation indicator (LED) is illuminating. (1) Broken connection of external load (2) Screws of terminal board are loose. (3) Pattern is broken.	Replace defective external load. Retighten screw terminals. Replace defective unit.
5	Output of specific relay No. does not turn off.	• Operation indicator (LED) is not illuminating. (1) Improper reset due to leakage current or saturation voltage.	Replace defective external load or add a dummy resistor.
		• Operation indicator LED is not illuminating. (1) Contact of jack is defective (bus line) (2) Relay Nos. of OUT instruction in the program are in duplication. (3) Power circuit is defective.	Clean with alcohol-moistened cloth. Correct the program. Replace defective unit.
6	Relay No. of abnormal operation is in units of 8. (Example) 0020, 0030	(1) Data bus signal is faulty.	Remove all the I/O units being used and insert them one by one to find the defective unit.
		(2) IC-RAM of CPU is defective.	Replace CPU rack.
7	Outputs turn on and off irregularly.	(1) Supply voltage of external load is low.	Raise the external supply voltage.
		(2) Relay Nos. of OUT instruction in the program are in duplication.	Correct the program.
		(3) Malfunction due to noise	Countermeasures against noise • Install a surge suppressor. • Install a insulating transformer. • Wiring with a shielded cable, etc.
8	Output operation indicator does not illuminate. (Operation is normal.)	(1) LED indicator is defective.	Since this type of defect does not impede normal operation, repair it in spare time or at the next periodic inspection.

Control I/O and DATA I/O Assignment Table for OMRON SYSMAC-M1R

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Relay No.	Description of signal	Relay No.	Description of signal
00		40	
01		41	
02		42	
03		43	
04		44	
05		45	
06		46	
07		47	
10		50	
11		51	
12		52	
13		53	
14		54	
15		55	
16		56	
17		57	
20		60	
21		61	
22		62	
23		63	
24		64	
25		65	
26		66	
27		67	
30		70	
31		71	
32		72	
33		73	
34		74	
35		75	
36		76	
37		77	

Timer/Counter Assignment Table for OMRON SYSMAC-M1R

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Relay No.	Description of signal	Relay No.	Description of signal
00		40	
01		41	
02		42	
03		43	
04		44	
05		45	
06		46	
07		47	
10		50	
11		51	
12		52	
13		53	
14		54	
15		55	
16		56	
17		57	
20		60	
21		61	
22		62	
23		63	
24		64	
25		65	
26		66	
27		67	
30		70	
31		71	
32		72	
33		73	
34		74	
35		75	
36		76	
37		77	

OMRON SYSMAC-M1R FAILURE/ABNORMAL MODE NO. LIST

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

FAL No.	Condition (Cause)	Countermeasure	FAL No.	Condition (Cause)	Countermeasure
00			50		
01			51		
02			52		
03			53		
04			54		
05			55		
06			56		
07			57		
08			58		
09			59		
10			60		
11			61		
12			62		
13			63		
14			64		
15			65		
16			66		
17			67		
18			68		
19			69		
20			70		
21			71		
22			72		
23			73		
24			74		
25			75		
26			76		
27			77		
28			78		
29			79		
30			80		
31			81		
32			82		
33			83		
34			84		
35			85		
36			86		
37			87		
38			88		
39			89		
40			90		
41			91		
42			92		
43			93		
44			94		
45			95		
46			96		
47			97		
48			98		
49			99		

OMRON SYSMAC-M1R CODING SHEET

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Program address	OP code	Relay No. (Data)	Remarks	Program address	OP code	Relay No. (Data)	Remarks
0				50			
1				51			
2				52			
3				53			
4				54			
5				55			
6				56			
7				57			
8				58			
9				59			
10				60			
11				61			
12				62			
13				63			
14				64			
15				65			
16				66			
17				67			
18				68			
19				69			
20				70			
21				71			
22				72			
23				73			
24				74			
25				75			
26				76			
27				77			
28				78			
29				79			
30				80			
31				81			
32				82			
33				83			
34				84			
35				85			
36				86			
37				87			
38				88			
39				89			
40				90			
41				91			
42				92			
43				93			
44				94			
45				95			
46				96			
47				97			
48				98			
49				99			

OMRON SYSMAC-M1R CODING SHEET

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Program address	OP code	Relay No. (Data)	Remarks	Program address	OP code	Relay No. (Data)	Remarks
000				050			
001				051			
002				052			
003				053			
004				054			
005				055			
006				056			
007				057			
008				058			
009				059			
010				060			
011				061			
012				062			
013				063			
014				064			
015				065			
016				066			
017				067			
018				068			
019				069			
020				070			
021				071			
022				072			
023				073			
024				074			
025				075			
026				076			
027				077			
028				078			
029				079			
030				080			
031				081			
032				082			
033				083			
034				084			
035				085			
036				086			
037				087			
038				088			
039				089			
040				090			
041				091			
042				092			
043				093			
044				094			
045				095			
046				096			
047				097			
048				098			
049				099			

OMRON SYSMAC-M1R CODING SHEET

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Program address	OP code	Relay No. (Data)	Remarks	Program address	OP code	Relay No. (Data)	Remarks
0				50			
1				51			
2				52			
3				53			
4				54			
5				55			
6				56			
7				57			
8				58			
9				59			
10				60			
11				61			
12				62			
13				63			
14				64			
15				65			
16				66			
17				67			
18				68			
19				69			
20				70			
21				71			
22				72			
23				73			
24				74			
25				75			
26				76			
27				77			
28				78			
29				79			
30				80			
31				81			
32				82			
33				83			
34				84			
35				85			
36				86			
37				87			
38				88			
39				89			
40				90			
41				91			
42				92			
43				93			
44				94			
45				95			
46				96			
47				97			
48				98			
49				99			

Authorized distributor: