Error Control

With the Processor, responsibility for error recovery rests with the host computer. The host computer controls the following error recovery procedures:

- When execution is impossible (end code) because of an undefined command error (header code) or setting, communication is terminated.
- If an error other than as described in 1 above occurs, a retry operation (re-transmission of the same command block) is executed.
- If no response block is returned within 5 seconds from the command block re-transmission, an error is assumed and a retry operation is executed.
- If an error occurs after three retry operations, communication is terminated.
- Note that when a Processor is connected to a system currently in use, the host computer of that system executes an error recovery operation.

The following error detection is performed at the Processor:

1, 2, 3... 1. Character check (check of every character)

- Vertical parity check (even parity). Exclusive OR (EOR) check for each character.
- Frame check. If a “0” is detected at the stop bit position, it is assumed that an error has occurred during communication.
- Overrun check. Overrun occurs when the next character is received while the current character is being processed.

2. Block check (check of each block)

- Format check. Command format construction is checked.
- Registration data check. Check of numerical range of numbers such as unit number and bank number.
- FCS check. Exclusive logical sumcheck of @ to the last text character.

If the above checks detect that an error has occurred during communication, error recovery control is requested at the host computer by the response block end code. Note, however, that when it is determined that the communication address is different through the registration data check, no response block is transmitted.